Calhoun
Institutional Archive of the Naval Postgraduate School

Calhoun: The NPS Institutional Archive

DSpace Repository

Theses and Dissertations | 1. Thesis and Dissertation Collection, all items

1993-03

Four frequency-shift keying (4-FSK) spread spectrum modulator and demodulator

Murray, Terrence J.

Monterey, California. Naval Postgraduate School

http://hdl.handle.net/10945/39876

This publication is a work of the U.S. Government as defined in Title 17, United States Code, Section 101. Copyright protection is not available for this work in the United States.

Downloaded from NPS Archive: Calhoun

http://www.nps.edu/library

Calhoun is the Naval Postgraduate School's public access digital repository for research materials and institutional publications created by the NPS community. Calhoun is named for Professor of Mathematics Guy K. Calhoun, NPS's first appointed -- and published -- scholarly author.

Dudley Knox Library / Naval Postgraduate School
411 Dyer Road / 1 University Circle
Monterey, California USA 93943

NAVAL POSTGRADUATE SCHOOL
Monterey, California

AD-A267 433

DTIC
ELECTE
AUG 0 4 1993
S A D

THESIS

FOUR FREQUENCY-SHIFT KEYING (4-FSK)
SPREAD SPECTRUM MODULATOR AND DEMODULATOR

by

Terrence J. Murray

March, 1993

Thesis Advisor: Tri T. Ha

Approved for public release; distribution is unlimited.

93-17365

REPORT DOCUMENTATION PAGE

1a Report Security Classification: Unclassified		1b Restrictive Markings	
2a Security Classification Authority		3 Distribution/Availability of Report	
2b Declassification/Downgrading Schedule		Approved for public release: distribution is unlimited.	
4 Performing Organization Report Number(s)		5 Monitoring Organization Report Number(s)	
6a Name of Performing Organization Naval Postgraduate School	6b Office Symbol *(if applicable)* EC	7a Name of Monitoring Organization Naval Postgraduate School	
6c Address *(city, state, and ZIP code)* Monterey CA 93943-5000		7b Address *(city, state, and ZIP code)* Monterey CA 93943-5000	
8a Name of Funding/Sponsoring Organization	6b Office Symbol *(if applicable)*	9 Procurement Instrument Identification Number	
Address *(city, state, and ZIP code)*		10 Source of Funding Numbers	
		Program Element No	Project No / Task No / Work Unit Accession No

11 Title *(include security classification)* FOUR FREQUENCY SHIFT KEYING (4-FSK) SPREAD SPECTRUM MODULATOR AND DEMODULATOR

12 Personal Author(s) Terrence J. Murray

13a Type of Report	13b Time Covered	14 Date of Report *(year, month, day)*	15 Page Count
Master's Thesis	From 07/90 To 03/93	March 1993	101

16 Supplementary Notation The views expressed in this thesis are those or the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

17 Cosati Codes			18 Subject Terms *(continue on reverse if necessary and identify by block number)*
Field	Group	Subgroup	

19 *Abstract*

This thesis explores the potential use of a four frequency-shift keying (4-FSK), spread spectrum modulator and demodulator (MODEM) in a low orbit satellite. In this first approach a short maximal length sequence of 127 chips would be used to spread the four frequencies. After successful implementation, the design could be extended to longer codes which would provide for greater processing gain. This MODEM was not preselected for use in satellite communications based on the merits of 4-FSK, but was assigned as one of four possible digital communication designs. A MODEM would be selected for use in the Petite Amateur Navy Satellite after a thorough design review.

20 Distribution/Availability of Abstract	21 Abstract Security Classification	
_X unclassified/unlimited __ same as report __ DTIC users	Unclassified	
22a Name of Responsible Individual Tri T. Ha	22b Telephone *(include Area Code)* (408) 656-2352	22c Office Symbol EC/Ab

DD FORM 1473,84 MAR 83 APR edition may be used until exhausted

All other editions are obsolete

Approved for public release; distribution is unlimited.

FOUR FREQUENCY-SHIFT KEYING (4-FSK) SPREAD SPECTRUM MODULATOR AND DEMODULATOR

by

Terrence J. Murray
Lieutenant Commander, United States Navy
B.S., Northern Arizona University, 1977

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March, 1993

Author: [redacted]
Terrence J. Murray

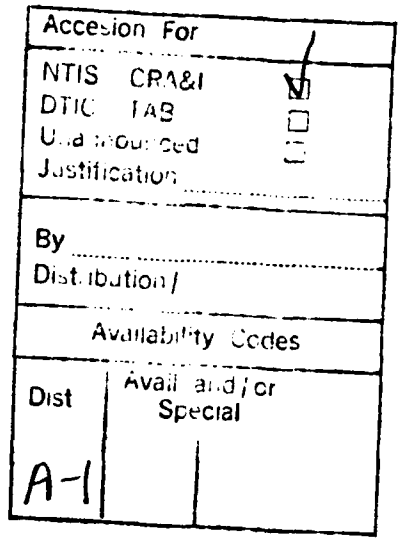
Approved by: [redacted]
Tri T. Ha, Thesis Advisor

[redacted]
Rudolf Panholzer, Second Reader

[redacted]
Michael A. Morgan, Chairman
Department of Electrical and Computer Engineering

ABSTRACT

This thesis explores the potential use of a four frequency-shift keying (4-FSK), spread spectrum modulator and demodulator (MODEM) in a low orbit satellite. In this first approach a short maximal length sequence of 127 chips would be used to spread the four frequencies. After successful implementation, the design could be extended to longer codes which would provide for greater processing gain. This MODEM was not preselected for use in satellite communications based on the merits of 4-FSK, but was assigned as one of four possible digital communication designs. A MODEM would be selected for use in the Petite Amateur Navy Satellite after a thorough design review.



DTIC QUALITY INSPECTED 3

TABLE OF CONTENTS

I. INTRODUCTION

The Petite Amateur Navy Satellite (PANSAT) concept calls for a low earth orbit satellite which provides digital, spread spectrum, store-and-forward, packet radio communication. PANSAT was originated by Professor Rudy Panholzer at the Naval Postgraduate School to provide the school's graduate students with an opportunity to apply classroom theory to a "real world" engineering project. To extend this opportunity to several communication graduate students, it was proposed that four modulators/demodulators (MODEMS) would be designed as independent thesis projects. The four MODEMS proposed are: binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), differential phase-shift keying (DPSK), and four frequency-shift keying (4-FSK).

The objective of this thesis is to design, build, and test a 4-FSK spread spectrum MODEM which could possibly be installed in PANSAT. The following initial parameters were provided as guidance in formulating the design:

1. noncoherent 4-FSK MODEM
2. spread spectrum using a maximal length spreading sequence (m-sequence) of 127
3. each data bit would be spread by one complete m-sequence
4. data bit spread would commence at the start of a chip (no single chip would span any two bit periods)

5. data bit rate equal to 1200 bits per second
6. spread spectrum channel bandwidth not to exceed 900 kHz
7. low power using CMOS technology
8. low orbit equal to 400 nautical miles

A design review would be held to determine which of the completed designs best meets the PANSAT requirements for size, weight, power consumption, cost, complexity (ability to duplicate the prototype), bandwidth and bit error rate.

II. Design Theory

A. 4-FSK SPREAD SPECTRUM MODULATION

1. General

The diagram of Figure 1 shows the Modulator Group consisting of the following three modules:

1. Serial-to-Parallel Conversion (M1)
2. Sine Wave Generation (M2)
3. Spread Spectrum (M3)

The theory considered during the design of each of these modules is discussed under separate sub-paragraphs of this chapter. A basic understanding of electronic circuit and

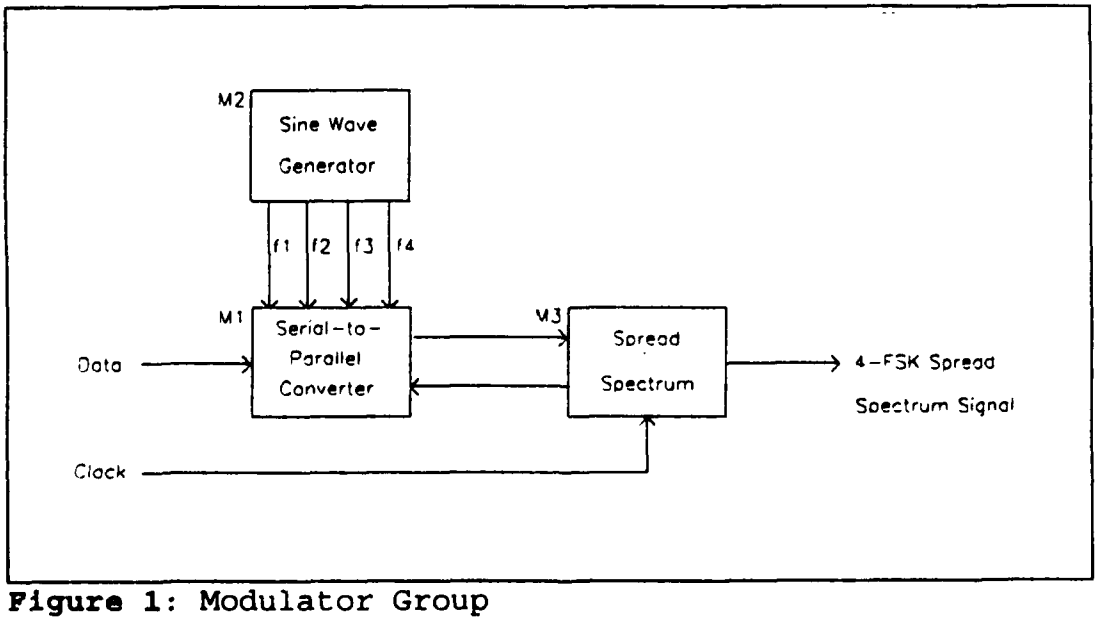


Figure 1: Modulator Group

spread spectrum theory is assumed. References 1, 2, and 3 should be reviewed for additional information concerning digital, analog, and spread spectrum engineering design respectively.

2. Serial-to-Parallel Data Conversion Module

Before the modulator's serial-to-parallel converter can be designed, consideration must be given to the method by which the demodulator will synchronize with the received signal. As a result of spread spectrum modulation, the demodulator must synchronize with the spreading m-sequence prior to data transmission. Because of this, the m-sequence was inspected for possible use in data synchronization. The digital logic sequence for a seven stage shift register with taps at stage three and seven is written out in Figure 2. From Figure 2 it was recognized that any successive grouping of

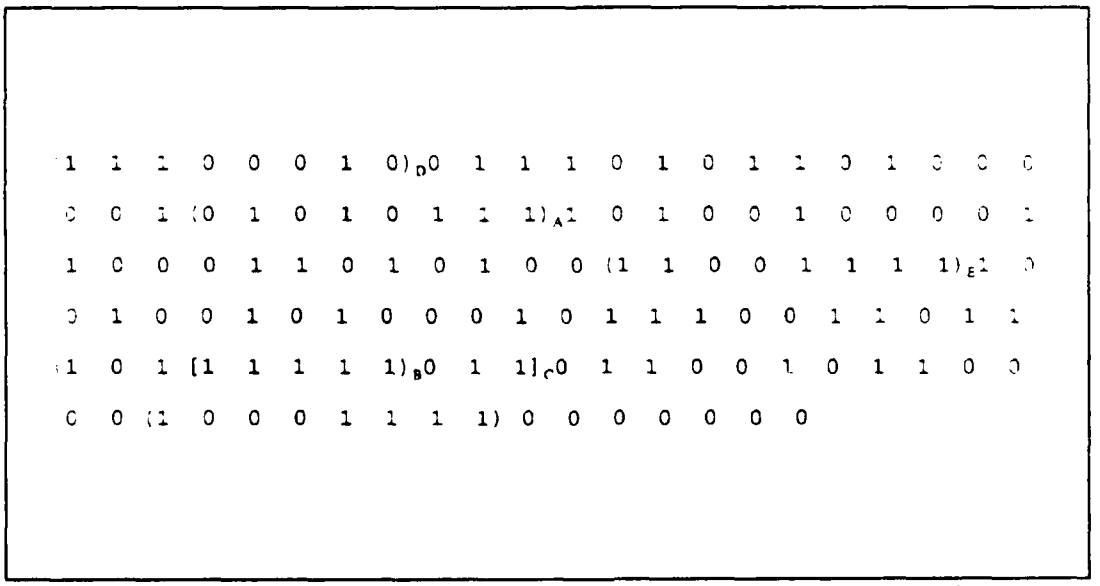


Figure 2. M-sequence, N = 127, taps at stage 3 and 7

seven chips from the total set of 127 chips was unique (not repeated). The serial-to-parallel converter module of Drawing A-1 utilizes eight chip m-sequence code bytes for data synchronization. By clearing the m-sequence shift register at the start of data transmission a reference would be established for clocking in serial data and clocking out a parallel symbol (two bits). From Figure 2 subscripted groups A and B are used to clock serial data into the serial input/parallel output shift register by clocking data in the middle of each serial data bit period. Subscripted group C latches a pair of bits into the decoder shortly after the second bit of the two bit pair is clocked into the shift register. Within 0.5μs a radio frequency (RF) pulse representing the bit pair which was latched into the decoder is switched to the output of the demodulator. For synchronization purposes at the demodulator, subscripted group C will signal the start of an RF pulse. The analog switch is a guaranteed "break before make" switch which results in only one of the four radio frequencies on the output line at any given time. All digital logic circuit set-up times were achieved by maintaining at least a one chip time interval between bit transfers.

To ensure that incoming data is synchronized to the shift register and decoder clocks two additional subscripted groups D and E should be created as outputs from the serial-to-parallel converter. These two pulses would be used to clock

the external data device thus ensuring that the serial input data is latched in the middle of the data period. Advantages to using the m-sequence to control synchronization are:

1. Deletes the requirement that the m-sequence shift register be cleared at the start of data transmission. This would eliminate a critical timing consideration and eliminate the potential for drift between two asynchronous timing waveforms.
2. Any chip rate can be selected.
3. The data rate will always be dependent on the chip rate.
4. Each data bit will always be sub-divided by one complete chip sequence.
5. The start of each RF pulse is known.
6. Each RF pulse can be further sub-divided into 127 equal parts.

3. Sine Wave Generator Module

The FSK signal can be generated in one of two ways as indicated in Figure 3. Either using a separate oscillator for each frequency and switching on the desired frequency or using a frequency modulator (voltage controlled oscillator) which is capable of producing multiple frequencies. With only four frequencies required to implement a 4-FSK modulator it is viable to build four separate sine wave generators or a single voltage controlled oscillator (VCO). In the case of higher order FSK modulators (16 or greater), it would be impractical to build 16 or more separate oscillators in which case a VCO would be a better choice. This design uses four separate

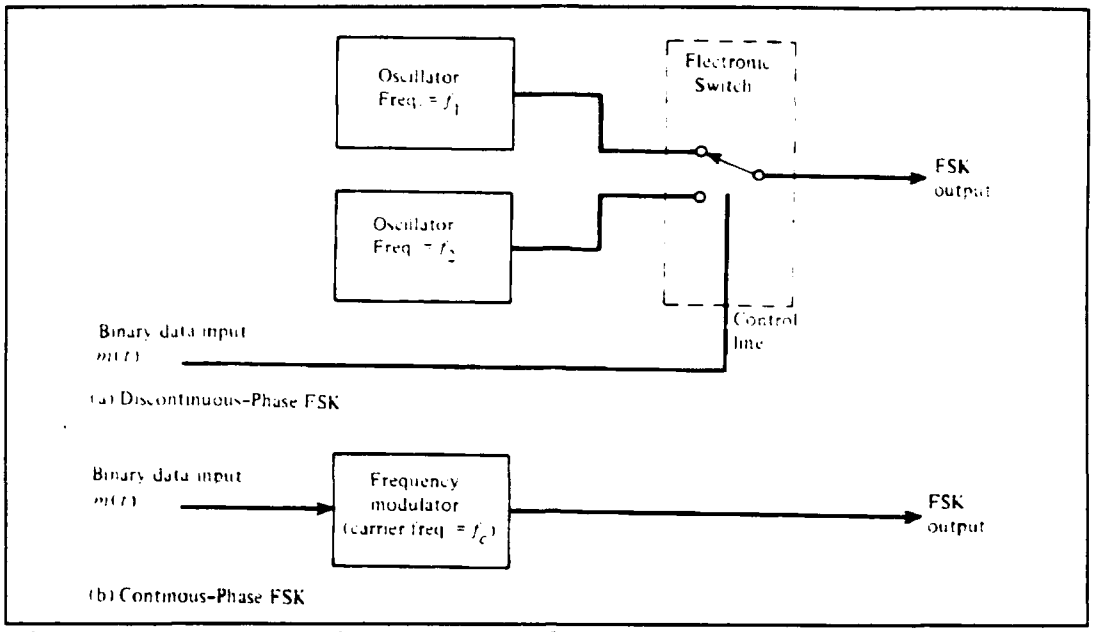


Figure 3. Generation of FSK [Ref. 4:p. 337]

precision sine wave generators which allows for precise frequency, maximum reduction of harmonic distortion, and second order low pass filters to significantly attenuate harmonics. A single VCO does not allow for this much control over the sine wave shape and would require additional switches to route each frequency as it is selected to the appropriate low pass filter.

For 4-FSK, four frequencies must be determined. The precision sine wave generator module of Drawing A-2 is limited to approximately 350 khz and active filter design is limited to approximately 500 khz. If square law detection was used then the lowest probability of bit error would result if and only if the frequencies were mutually orthogonal. This means

that the change in one frequency to another is an integer multiple of the bit rate (R_b).

$$\Delta f = \frac{n}{T_b} = nR_b \qquad n = 1,2,3, \cdots$$

The bit rate of the data is 1200 bits per second but in 4-FSK modulation this is reduced to a symbol rate (R_s) of 600 symbols per second.

$$\Delta f = \frac{n}{T_s} = nR_s$$

In this spread spectrum modulation scheme, each symbol is sub-divided by the length of one entire m-sequence which for this design is equal to 127 chips.

$$\Delta f = \frac{n}{T_s/127} = 127nR_s$$

Using the requirement for mutually orthogonal sinusoids, Rs = 600, and n = 1, 2, 3, and 4, the four frequencies are: f1 = 76.2 khz, f2 = 152.4 khz, f3 = 228.6 khz, and f4 = 304.8 khz.

Square law detection only works if the channel frequencies are constant values. An orbiting satellite whose position changes with time in relation to a site on earth creates a doppler shift which causes the channel frequencies to continually vary. Due to varying channel frequencies, the demodulator was designed using envelope detectors. Envelope detectors do not require that the FSK frequencies be mutually orthogonal, but that they are far enough apart in the

frequency domain so that one frequency does not get mistaken for another. Since 4-FSK is simply a series of independent RF pulses, frequency separation can be determined by viewing the frequency domain of a single RF pulse, g(t).

$$g(t) = P\ rect(\frac{t}{T})\ \cos(2\pi f_o t)$$

Figure 4 is the time domain plot of the RF pulse. The Fourier Transform of g(t) is G(f).

$$G(f) = \frac{PT}{2}(sinc[T(f-f_c)] + sinc[T(f+f_c)])$$

Figure 5 is the frequency domain magnitude plot of G(f). Note from Figure 5 that the RF pulse has a main lobe bandwidth equal to twice the inverse of the RF pulse period (T). For a spread spectrum signal, the RF pulse phase is no longer constant but is changed according to the m-sequence. When the RF pulse period (T) is segmented into 127 parts (number of chips in the m-sequence), the resultant RF pulse period is reduced to a new, shortened period, called the chip period (T_c). Substituting T_c for T in Figure 5 results in the frequency spectrum magnitude plot of Figure 6. The bandwidth is still equal to twice the inverse of the RF pulse period. Only now the pulse period is the shorter chip period (T_c), and the bandwidth is widened in proportion to the length of the m-sequence.

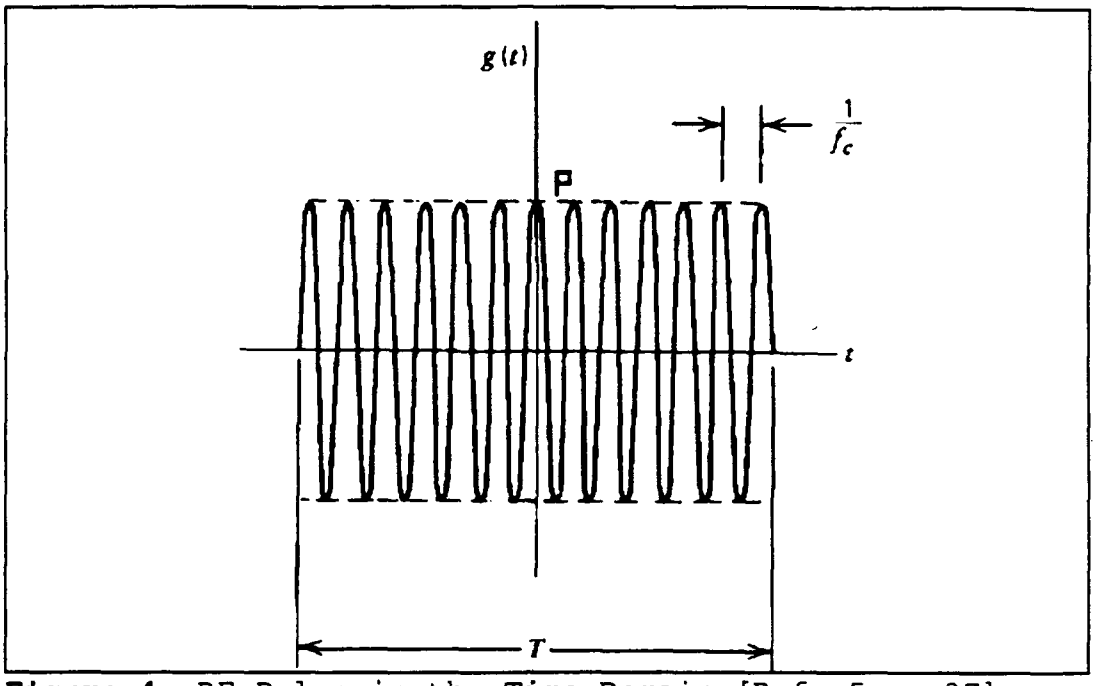


Figure 4: RF Pulse in the Time Domain [Ref. 5:p. 37]

A minimum channel frequency separation for a spread spectrum

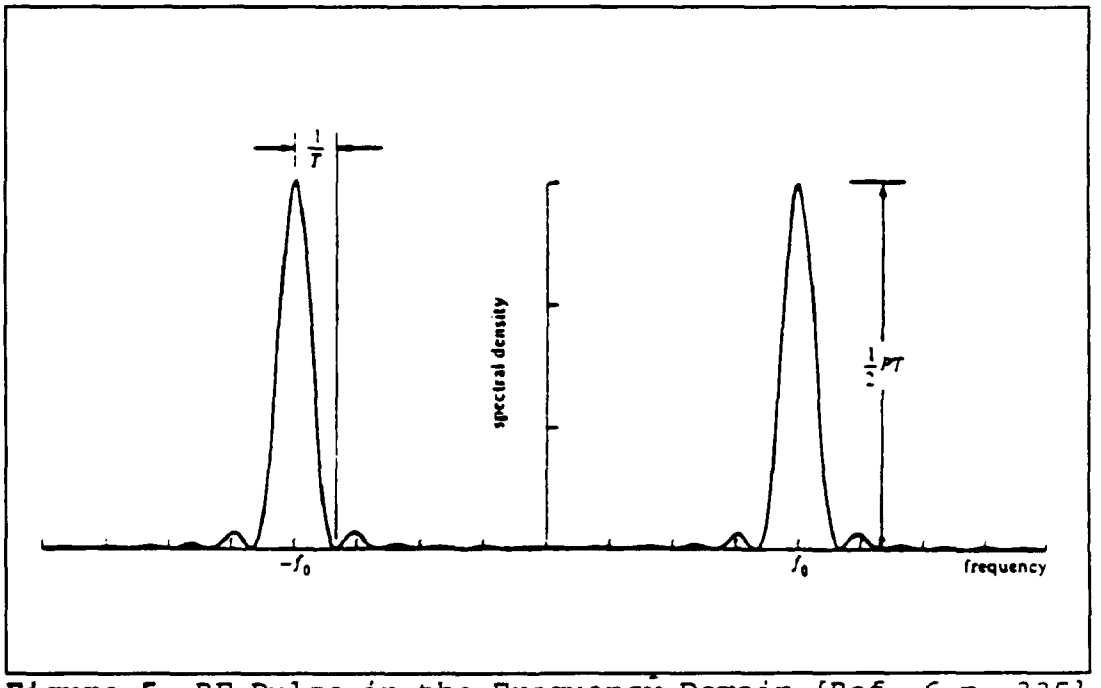


Figure 5: RF Pulse in the Frequency Domain [Ref. 6:p. 335]

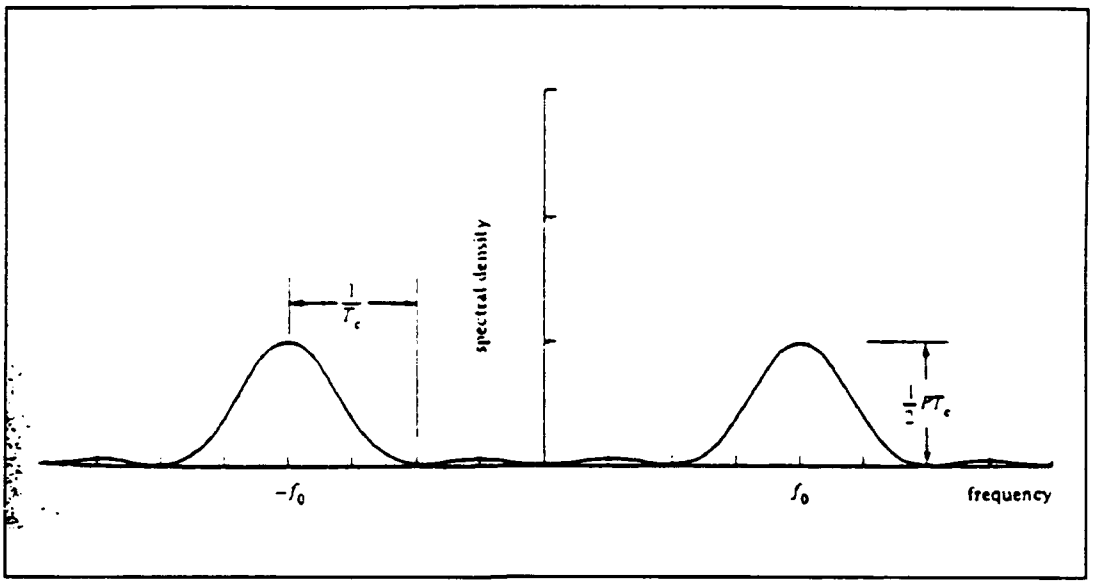


Figure 6: Spread Spectrum RF Pulse in the Frequency Domain [Ref. 6:p. 335]

$$Spread\ Spectrum\ BW = \frac{2}{T_c} = \frac{2}{T/127} = 152.4\ kHz$$

demodulator which uses envelope detectors is one half the spread main lobe bandwidth or 76.2 khz. The modulator frequencies of 76.2 khz, 152.4 khz, 228.6 khz, and 304.8 khz were selected. These frequencies are within the range of the sine wave generators, can be shaped with active filters, and meet the minimum separation requirements.

The low pass filters are 2nd order GIC filters. All active filters used in both the modulator and demodulator are GIC filters and are covered as a separate topic in Appendix B.

All buffers used in both the modulator and demodulator were constructed using LM318 operational amplifiers because of the component's high slew rate (70 V/μs) and wide bandwidth (15 Mhz). These are covered as a separate topic in Appendix C.

4. Spread Spectrum Module

The spread spectrum module, M3, of Drawing A-3 is comprised of a code sequence generator, a doubly balanced mixer, and a buffer. Using Table 8-5 of [Ref. 6:pp. 390-391], the generator polynomial for an m-sequence of length 127 is $g(D) = 1 + D^3 + D^7$. The powers of the generator polynomial determine the final form of the General Multiple-Tap Simple Sequence Generator (SSRG) of Figure 7. The SSRG circuit is implemented by connecting the third (D_3) and seventh (D_7) stage outputs of an eight stage shift register to an exclusive-nor gate and back to the shift register's first stage data input. The sequence can be tapped off of any of the shift register's eight outputs (Q1 through Q8). An eight input nand gate prevents the generator from locking-up with all ones (high

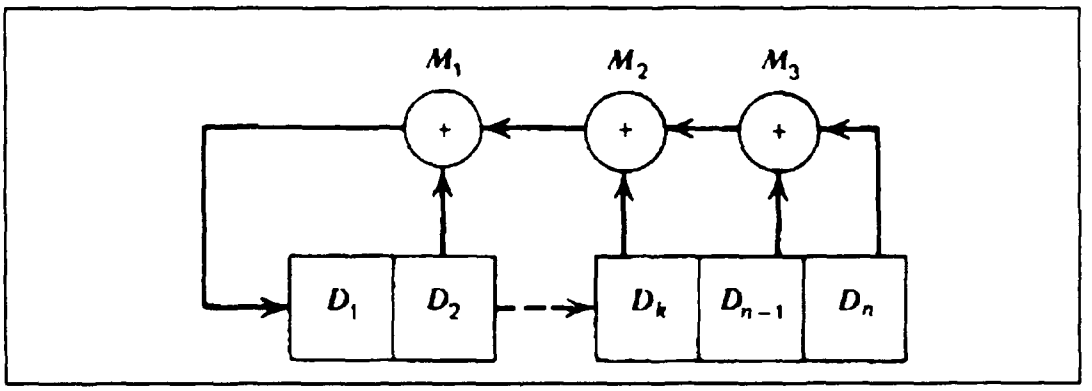


Figure 7. Multiple-tap simple sequence generator (SSRG) [Ref. 3:p. 68]

digital value equal to a nominal plus five volts). If at start-up or due to noise all of the outputs are one, the

output of the nand gate will be zero (low digital value equal to a nominal zero volts) and will clear the shift register to all zeros and re-start the m-sequence. In order to introduce phase changes and not imbalance the amplitude of the output sinusoid, the spreading m-sequence must alternate between positive and negative voltages of equal amplitude rather than the nominal zero to five volt digital logic output of the shift register. This is accomplished by connecting the output of the shift register to a comparator whose reference voltage is set at a mid-point value between zero and five volts. The comparator voltage supplies are adjusted so that the output voltage swings between positive and negative values of equal amplitude (A). Hence as the digital logic m-sequence changes logic levels, the comparator output voltage changes between ±A.

The doubly balanced mixer (DBM) multiplies the two inputs. The output is one of the four symbol frequencies but instead of being at a constant phase during its pulse duration its phase now varies with the change of phase of the m-sequence. This has the effect on the amplitude and bandwidth of the frequency domain signal as shown in Figure 6. The amplitude is reduced and the bandwidth is increased proportional to the length of the m-sequence.

B. 4-FSK Spread Spectrum Demodulation

1. General

The diagram of figure 8 shows the 4-FSK demodulation grouped into the following six modules:

1. Band Pass Filter (M4)
2. Decision Making (M5)
3. Frequency Sweep (M6)
4. Early Minus Late (M7)
5. Track (M8)
6. Synchronization (M9)

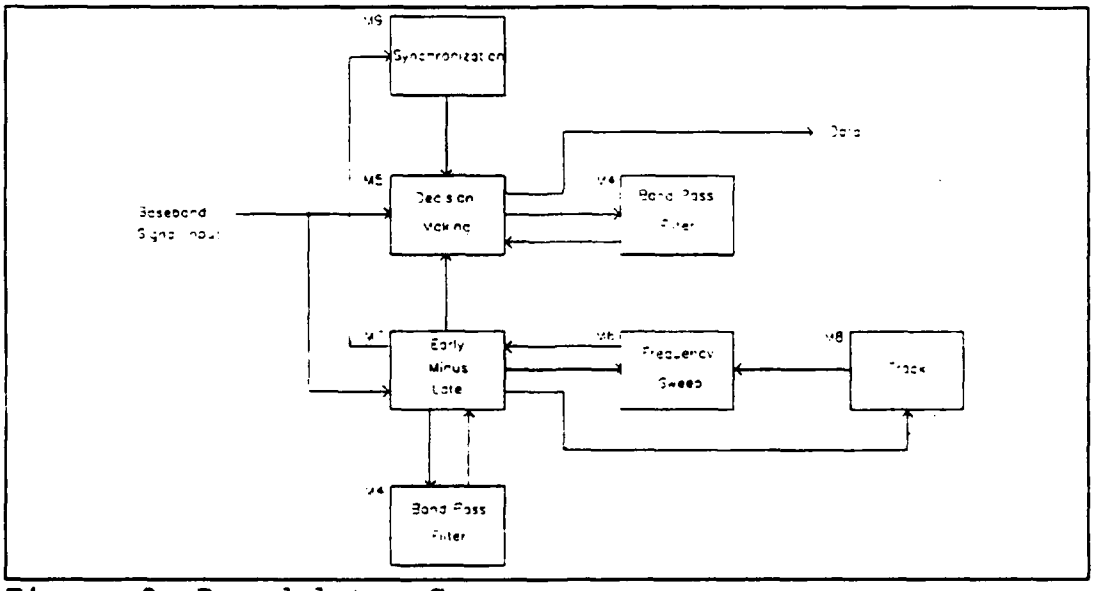


Figure 8. Demodulator Group

Module M5 with some additional synchronization circuitry is the only module required if spread spectrum had not been employed. The other three modules are all involved in acquiring/tracking the m-sequence used to despread the received signal and provide synchronization to the decision making module.

2. Band Pass Filter Module

Identical sets of band pass filters are used in the decision making circuitry prior to envelope detection and in the early minus late acquisition circuitry. These applications will be discussed separately. This section covers band pass filter design.

The 4th order band pass filters were designed by cascading two Generalized Impedance Converter (GIC) second order active filter networks. The center frequency for each of the band pass filters is equal to the channel frequency as determined in paragraph II.A.3. To find the upper and lower 3dB frequencies, the frequency shift from the center frequencies due to worst case doppler shift and the main lobe bandwidth of the despread channel frequencies must first be calculated. The worst case doppler shift as calculated in Appendix D is 9784 Hz. Adding one-half the channel bandwidth to the maximum doppler shift frequency results in 10,384 Hz as the amount that must be added and subtracted from each of the center frequencies to calculate the upper and lower 3dB

frequencies respectively. The design criteria for each of the four band pass filters is listed below:

Q	center freq(Hz)	lower 3dB freq(Hz)	upper 3dB freq(Hz)
3.67	76,200	65,816	86,584
7.38	152,400	142,016	162,784
11.00	228,600	218,216	238,984
14.68	304,800	294,416	315,184

Each band pass filter was designed using the procedure in Appendix B. Magnitude plots of the band pass filters using the passive elements of Drawing A-4 are shown in Figures 9 through 12 for channel frequencies 76.2kHz through 304.8kHz respectively.

3. Decision Making Module

As previously discussed in paragraph II.A.3., demodulation would be accomplished using envelope detectors. The block diagram of a two channel noncoherent FSK demodulator is shown in Figure 13. Any higher order m-ary FSK demodulator can be designed by duplicating the building blocks of Figure 13 once for each additional pair of transmission channels. The 4-FSK decision making module comprised of filters, amplifiers, envelope detectors, integrators, and decision making circuitry is shown in Drawing A-5.

The gain of the amplifiers at the output of the band pass filters was determined on the constructed circuit by inserting each of the four channel frequencies (all of two

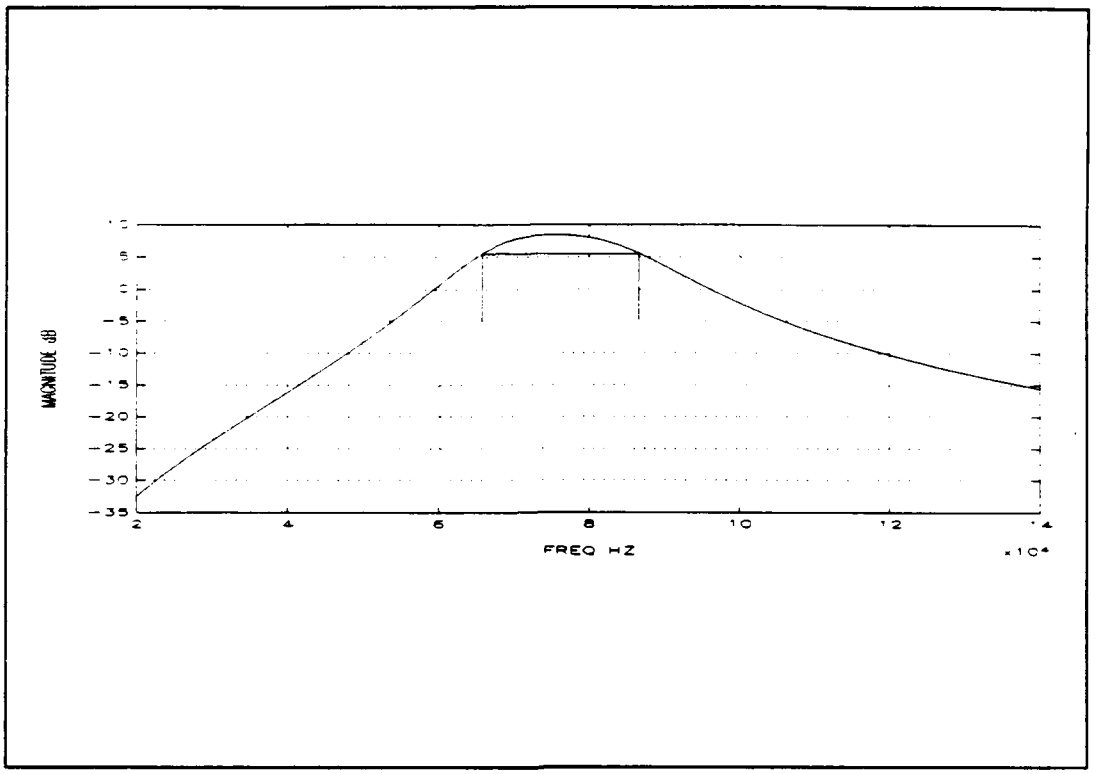


Figure 9. 4th Order BPF, f_0 = 76.2 kHz, Q = 3.66

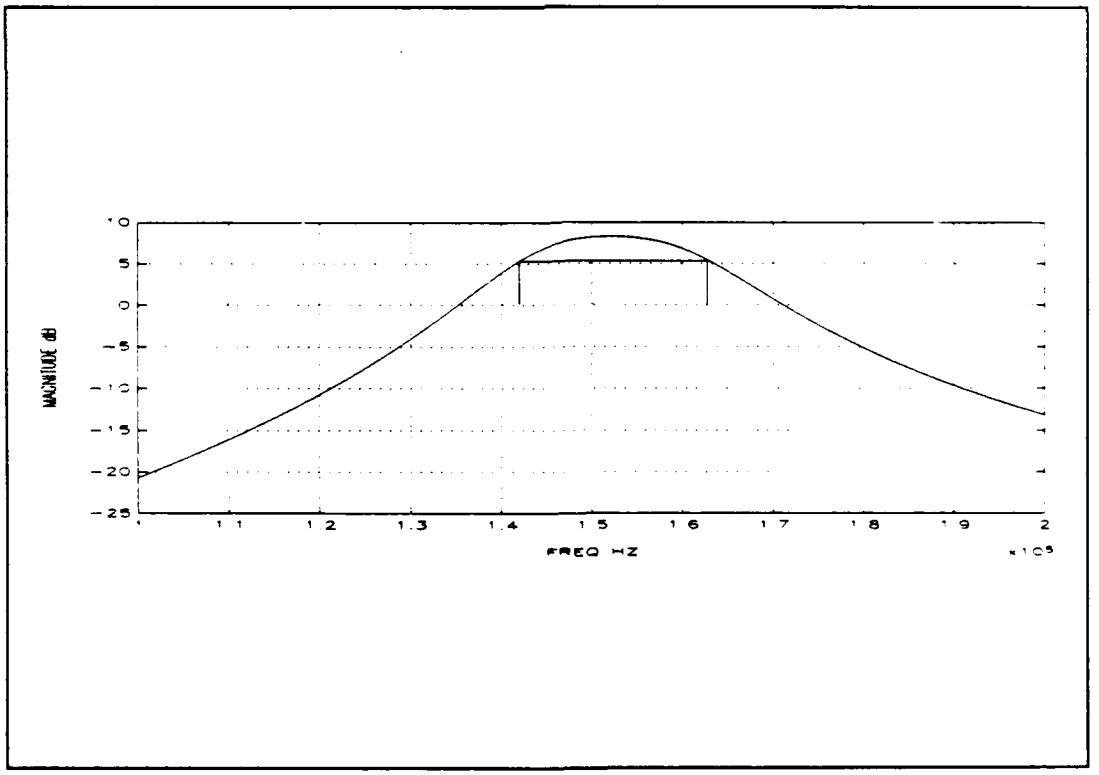


Figure 10. 4th Order BPF, f_0 = 152.4 kHz, Q = 7.50

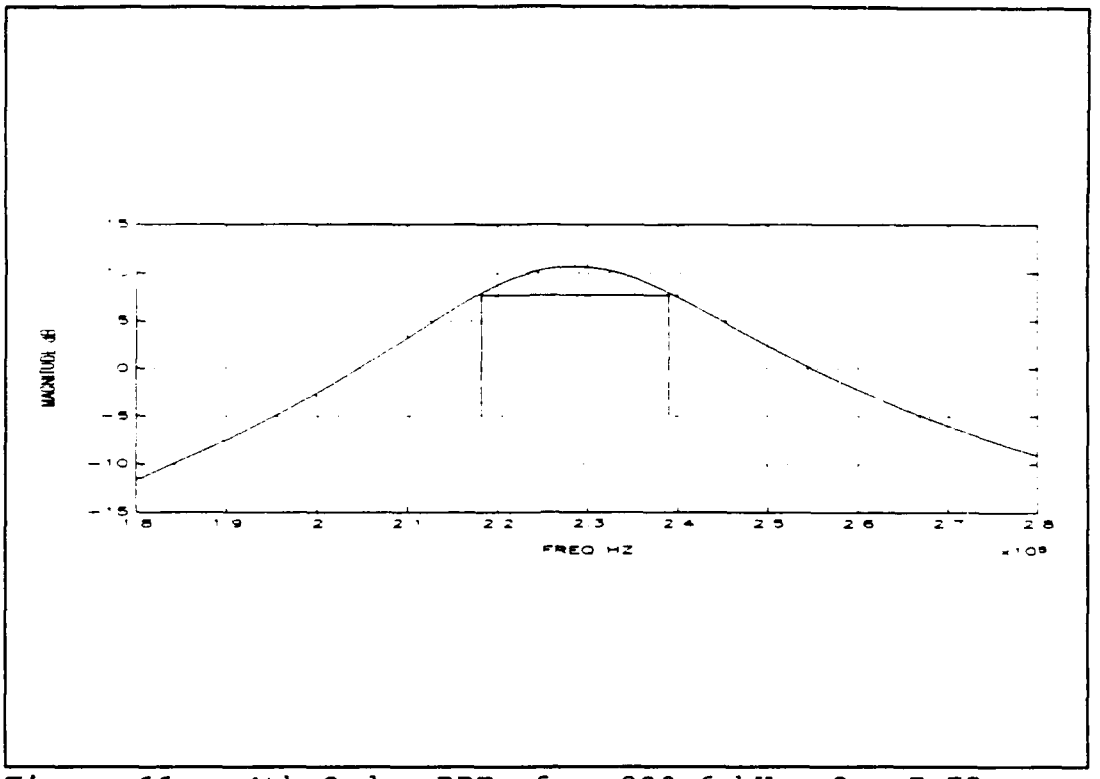


Figure 11. 4th Order BPF, f_0 = 228.6 kHz, Q = 7.75

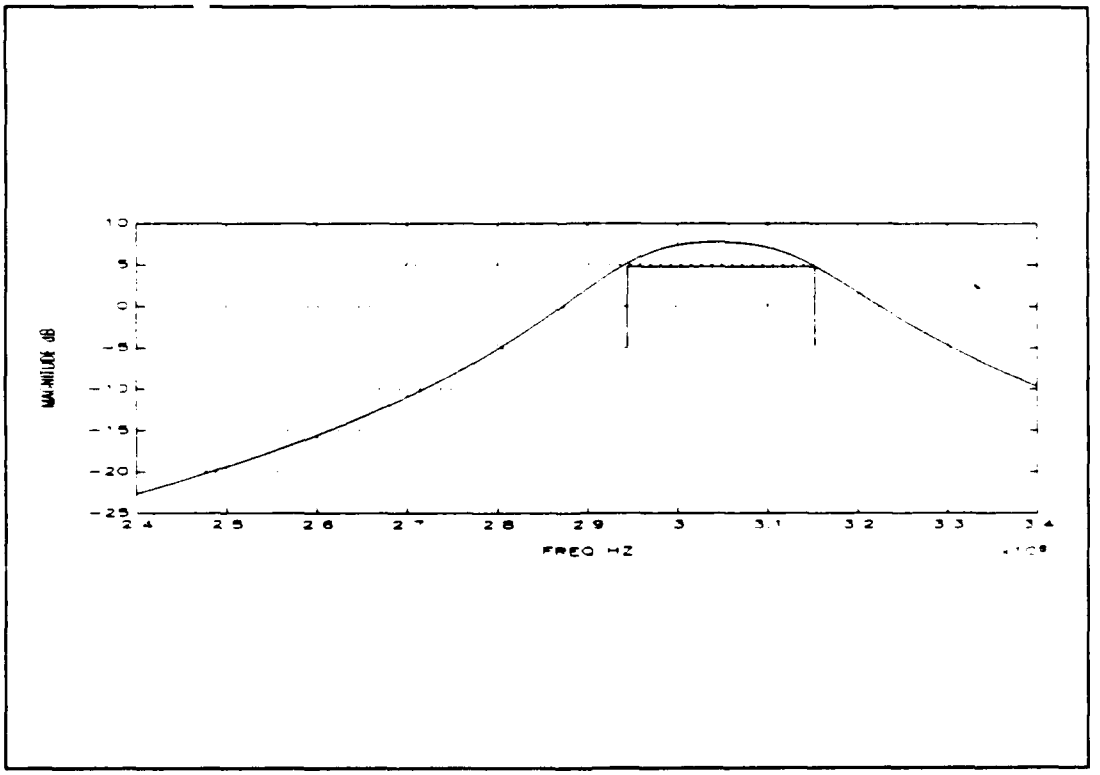


Figure 12. 4TH Order BPF, f_0 = 304.8 kHz, Q = 15.0

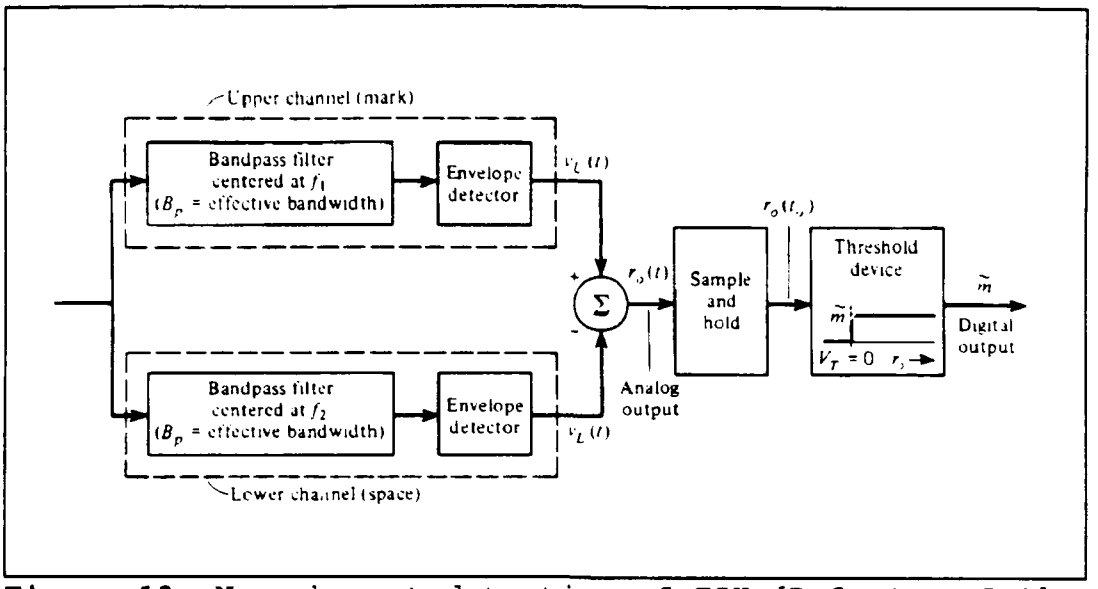


Figure 13. Noncoherent detection of FSK [Ref. 4:p. 543]

volts peak-to-peak) into their respective band pass filters and calculating the gain required to have a 12 volt peak-to-peak signal out of each of the amplifiers. This was done so that each transmitted channel when received by the envelope detector has equal weight in the decision making process.

The design of the envelope detectors was taken from [Ref. 5:pp. 272-273] but unlike envelope detectors for amplitude demodulation, the charging and discharging time constant, RC, must both be relatively short compared to the symbol duration. To keep subsequent integrations mutually independent, the stored energy in the envelope detector must be zero prior to the start of an integration. This requires that the capacitor voltage approach zero before the next integration begins. A simple passive low pass filter with a 1600 Hz cut-off frequency was placed after the envelope

detector to remove the high frequency ripple. The integrator was designed to ramp up in its nearly linear region during the symbol period, be sampled at the end of the symbol period where the maximum amount of signal energy could be captured, and dumped at the start of the next symbol. The integrator amplifier buffers the integrator from the comparator circuit that follows and also amplifies the integrator voltage which increases the likelihood that the comparators will correctly choose the integrator with the greatest signal energy.

A decision must be made as to which frequency is being received and then decoded to its two bit symbol representation. Once the bit pair is known, the pair must be separated and emitted from the module one bit at a time just as it was fed into the modulator at the transmission site. The decision criteria is simple. If f1 integrator voltage is greater than f2, f3, and f4 integrator voltages when compared on an individual basis then f1 was received. When this comparison is made for all four possible combinations only one frequency can be chosen as the received frequency. Given four frequencies, six comparators are required to implement all possible combinations (1 and 2, 1 and 3, 1 and 4, 2 and 3, 2 and 4, and 3 and 4). There are actually 12 permutations but since the other six are inverse relationships these comparisons can be achieved by inverting the comparators' output. Combinations of these 12 results are connected to the four three-input nand gates where an all high input drives the

appropriate priority encoder pin low which in turn activates one of the four bit pairs (00, 01, 10, 11). This comparison is done on a continuous basis and is only optimized to be correct at the end of the integration process. The synchronization which determines when to accept these comparisons is discussed in the demodulator synchronization module section. The bit pair is clocked into a parallel-to-serial shift register and then clocked out at twice the symbol rate.

4. Frequency Sweep Module

Not knowing the exact frequency and phase of the received m-sequence requires that the demodulator sweep through the range of all possible frequencies while looking for the correct one. The purpose of the frequency sweep module is to sweep through its range of frequencies until signaled by the early minus late module that the frequency is close enough to the received frequency to be acquired/tracked and that the phase of the received spreading m-sequence and demodulator despreading m-sequence match within one-half of a chip. This is summarized by the algorithm of Figure 14. Initial efforts to design an analog frequency sweep were unsuccessful because once the fixed analog voltage level required to drive the voltage controlled oscillator (VCO) was determined, it could not be held constant. Attempts to hold the voltage on low leakage polypropylene capacitors buffered by low input bias current (50pF) JFET operational amplifiers failed due to a

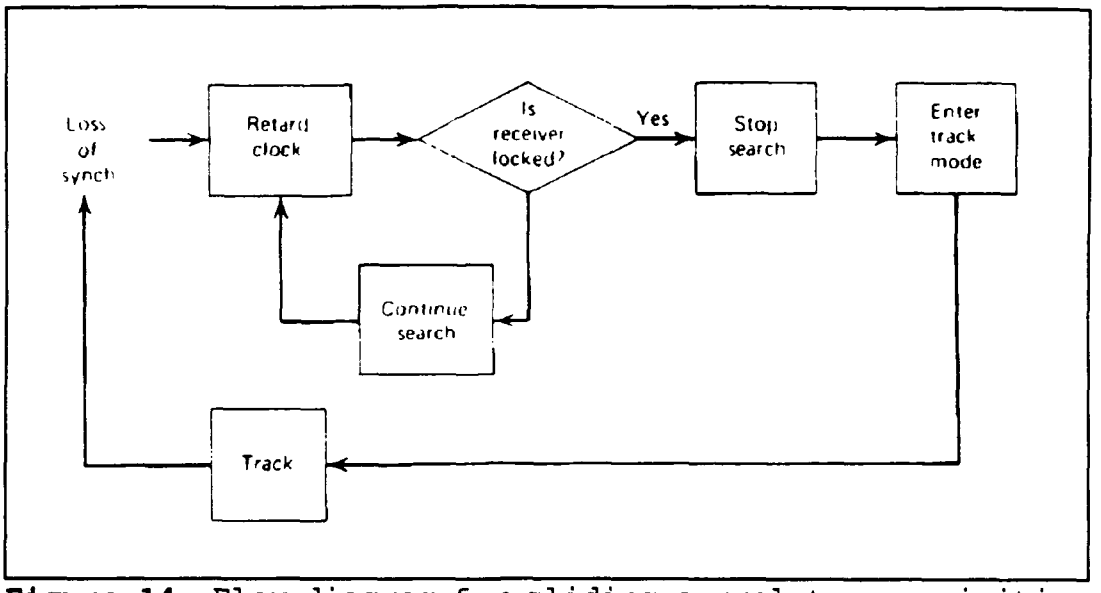


Figure 14. Flow diagram for sliding correlator acquisition [Ref. 3:p. 219]

slow discharge of the capacitors resulting in an unacceptable drift of the JFET output voltage. To correct for the inevitable discharge of the capacitor a refresh loop was installed to recharge the capacitor with the correct voltage level. This did not work because the operational amplifiers utilized in the refresh loop induced their own voltage drift due to the minute offset voltages which could not be completely removed. Therefore, the design shown in Drawing A-6 was developed using digital components. The eight bit counter steps through all 256 states, one state change for every positive-going clock pulse. The eight bits of each state are then clocked into an eight bit latch on every negative-going clock pulse. The one-half clock period delay assures that the 25ns set-up time is met. The digital-to-analog converter (DAC) produces incremental voltages based on the digital input which

in turn steps the VCO through the range of possible frequencies. This method works very well. Once the frequency sweep module is signaled to stop clocking, the latch holds the correct digital code indefinitely. The latched code drives a DAC whose output voltage is held constant by the use of its own voltage regulator. It is this well regulated voltage which locks in the frequency output of the VCO.

5. Early Minus Late

The concept behind the early minus late module is to provide the frequency sweep and track modules with the following information:

1. it signals when both the received m-sequence frequency approximately equals the demodulator m-sequence frequency to within plus or minus 100 Hz and the two m-sequences are in-phase.

2. provides feedback so that the final frequency adjustments can be made and the two frequencies remain in-phase within plus or minus one-half of a chip.

Early refers to an m-sequence which is advanced by one-half a chip in time ahead of the punctual (spreading) m-sequence and late refers to an m-sequence which is delayed by one-half of a chip in time behind the punctual m-sequence. The autocorrelation function (ACF) of these two m-sequences with the punctual m-sequence is plotted in the upper two graphs of Figure 15. The ACF term is used because in this context the two m-sequences are identical. Note that the ACF is approximately zero (equal to -1/127) everywhere except where

the m-sequences are within one chip of being in phase. Drawing A-7 shows the early minus late circuit. The early/late code sequence generator is identical to the modulator's code sequence generator of Drawing A-3 except for the addition of one shift register and one comparator. The shift register taps the digital logic m-sequence one full chip ahead of the punctual m-sequence and then by use of an inverted clock pulse advances the full chip early by one-half chip (early) and by one and one-half chips (late). There are now three digital m-sequences: punctual at the output of the upper (eight stage) shift register pin 4, one-half chip early at the output of the lower (four stage) shift register pin 5, and one-half chip late at the output of the lower (four stage) shift register pin 4. The comparators convert the early and late digital m-sequences to analog (±A constant voltage amplitude) m-sequences for reasons explained in paragraph II.A.4. Early minus late refers to the difference of the one-half chip early m-sequence autocorrelated with the punctual m-sequence and the one-half chip late m-sequence autocorrelated with the punctual m-sequence. In Figure 15 the top waveform is the early ACF, the middle waveform is the late ACF, and the bottom waveform is the early ACF minus the late ACF waveform. Using the block diagram of a full-time early-late noncoherent code tracking loop of Figure 16, a two channel loop was built. A two channel loop introduces problems in trying to precisely amplitude balance the early and late channels [Ref. 6:p. 447].

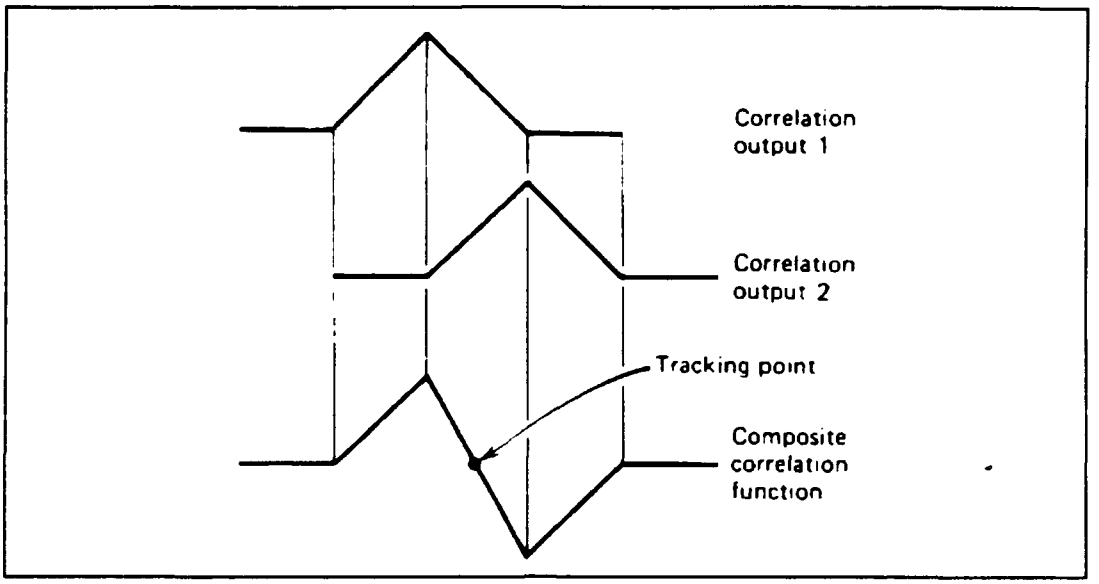


Figure 15. Autocorrelation Waveforms [Ref. 3:p. 254]

Specifically, it was found to be most difficult to build band pass filters with identical transfer functions. Even though great care was taken to match the values of the passive elements, the transfer functions were not the same. Additional work would be required to find operational amplifiers with matching small signal bandwidths. This was not done. Instead it was decided that it would be easier, use fewer components, and be more accurate to use a single channel and switch the ACF through one set of band pass filters thus assuring that both the early and late autocorrelation function products would be acted upon by the same band pass filter transfer function. The Tau dither early-late noncoherent code tracking loop of Figure 17 was used as a model for the modified single channel design of Drawing A-7. To more easily understand the circuit, the early autocorrelation and identification process

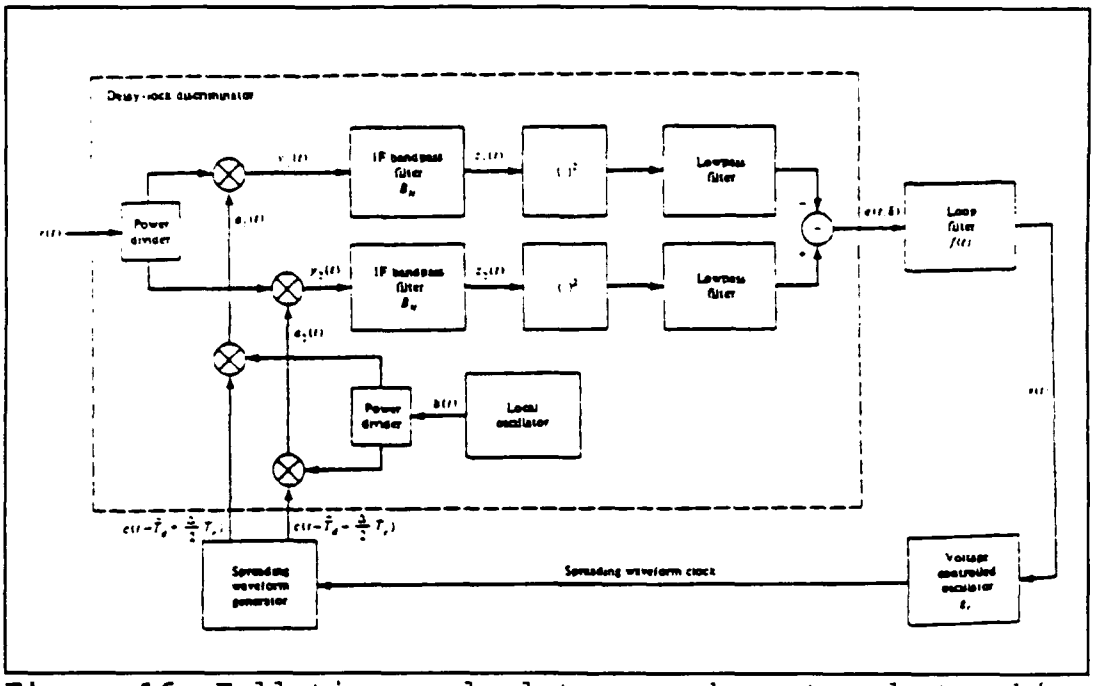


Figure 16. Full-time early-late noncoherent code tracking loop [Ref. 6:p. 434]

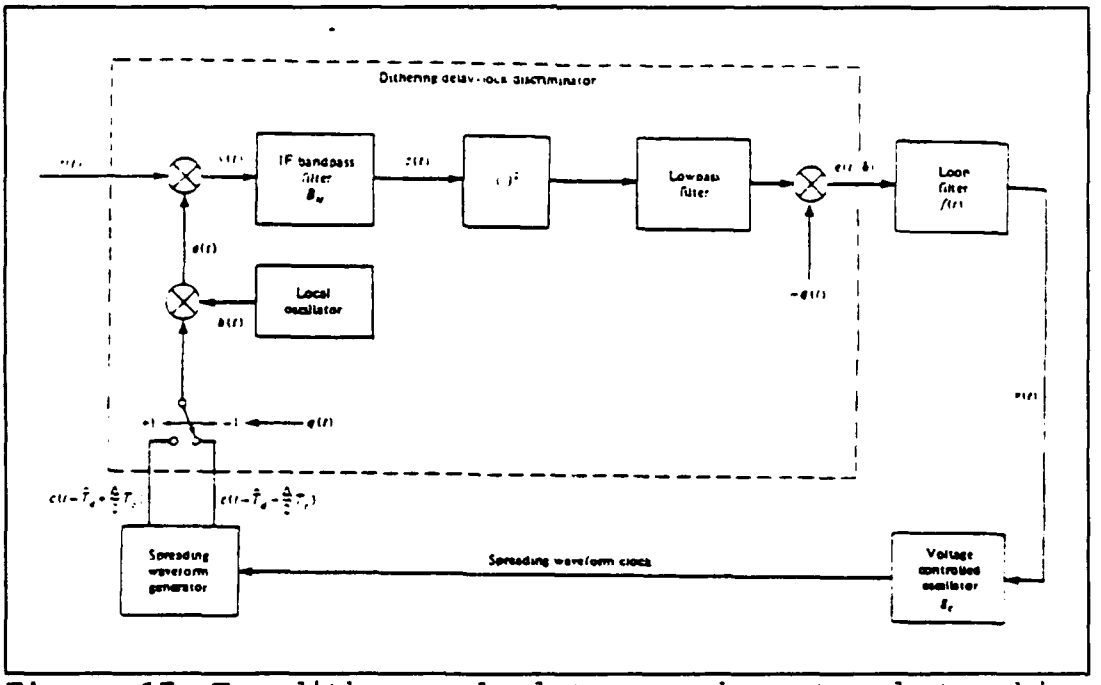


Figure 17. Tau-dither early-late noncoherent code tracking loop [Ref. 6:p. 448]

will be explained; the late autocorrelation and identification process is identical with the exception that the autocorrelation function (ACF) is inverted by reversing the envelope detector diode. The doubly balanced mixer multiplies the early analog m-sequence with the received spread spectrum signal and via switch SW-06 routes the product (ACF) to a bank of band pass filters identical to the ones used in the conventional demodulator of Drawing A-4. When each RF pulse is spread (see Figure 6), the spectral density found within the pass band of the band pass filter is reduced. As the m-sequences begin to correlate the spectral density begins to collapse about the RF pulse's center frequency until the two sequences are perfectly correlated. At this point in time, spectral density is at its greatest (Figure 5); therefore, there exists a direct relationship between spectral density and m-sequence autocorrelation. The early minus late module uses this relationship to provide voltage feedback to the frequency sweep and track modules. The magnitude of the spectral density of interest is found by passing the ACF through all four band pass filters, summing the output waveforms, and connecting the sum to an envelope detector. Since it is the change in magnitude in the pass band that is used as feedback, the DC offset is removed and the change in magnitude is amplified. The early ACF and the inverted late ACF are summed together to get the output of the discriminator of Figure 17. The modified loop filter is a lag RC filter

designed according to Figures 18 and 19 to reduce high frequency response. "Output signal-to-noise ratio can be significantly improved by this simple addition, which also decreases loop jitter with noisy input signals." [Ref. 3:p. 189] The voltage output of the loop filter is connected to the summing amplifier in the frequency sweep module via a voltage divider (variable resistor). Through experimentation, it was found that an approximately 40 mV peak-to-peak feedback control voltage locked the two m-sequences together. Larger feedback voltages caused ex sive jitter and lower feedback voltages would fail to lock the m-sequences together.

To signal the change from the acquisition mode to the track mode, two comparators were used to monitor the early and late ACF voltages. As both the early and late ACF voltages exceeded their reference voltages (plus and minus one volt respectively), the comparator outputs would go high. By looking at the ACF voltage waveforms of Figure 15, the only

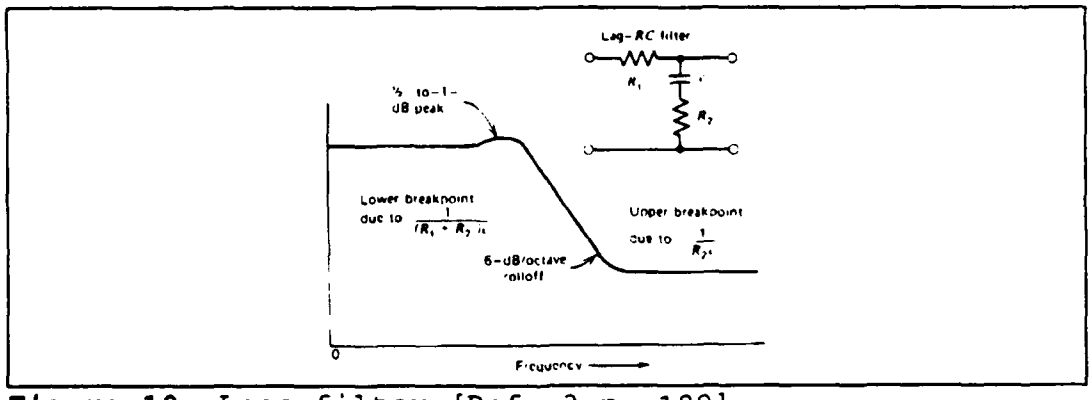


Figure 18. Loop filter [Ref. 3:p. 189]

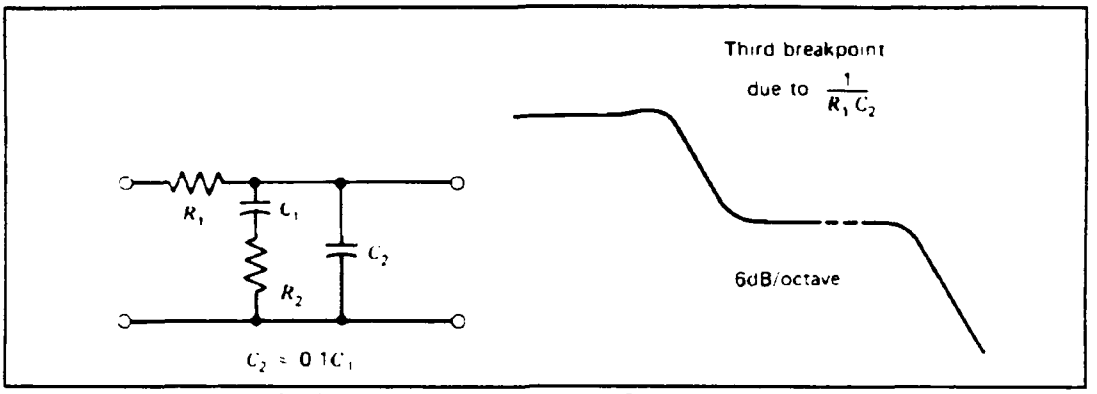


Figure 19. Modified loop filter [Ref. 3:p. 190]

time both the early and late ACF voltages are greater than zero is when the composite (early minus late) correlation function is in the linear region about the tracking point. When the and gate goes high, the counter which drives the DAC and VCO freezes the current value of the byte indicating that the VCO is close to the received m-sequence frequency. The feedback control voltage is then able to make the small adjustments necessary to maintain a lock on the received m-sequence frequency and phase. Because the spreading and despreading m-sequence frequencies were not perfectly matched, a DC offset to the composite correlation function of Figure 15 results. It is this DC offset that will be used as feedback to track frequency drift and doppler shift.

6. Track

If the transmitter and receiver were stationary, then there would be a relative velocity and doppler shift equal to zero. In this instance, the early minus late feedback voltage would provide all the necessary control to maintain

correlation between the spreading and despreading m-sequences. The relative velocity, however, is not equal to zero. Without a means of adjusting the average feedback voltage to zero, the DC offset would continue to increase (either negatively or positively depending on whether the doppler shift increased or decreased the frequency of the spreading m-sequence frequency) until it exceeded the range of feedback voltages. Two adverse events occur as the DC offset voltage increases:

1. The m-sequences will move further out of alignment resulting in a smaller signal-to-noise ratio and a higher bit error rate.

2. Acquisition will be lost prior to successful receipt of the entire information packet.

To track the doppler shift, a second feedback loop is created which will monitor the DC offset of the early minus late feedback voltage and adjust the digital code which ultimately determines the base frequency of the despreading m-sequence. When the frequency of the two m-sequences are equal, the DC offset of the control voltage waveform is zero. For a spread spectrum communication system which must correct for doppler shift, the goal is to keep the early minus late DC offset as close to zero as possible, thus overcoming both adverse effects of reduced signal-to-noise ratio and short acquisition times.

For optimum results, the early minus late feedback voltage should be sent to integrate, sample, and dump

circuitry to determine the average DC offset. The crude design of Drawing A-8 randomly samples the feedback voltage 30 times per second and compares the sample to zero volts. If the sample value is greater than zero, the comparator output goes low and then the byte 0000 0001 is added to the current byte which is driving the DAC. When the arithmetic logic unit (ALU) adds 0000 0001, it is the same as adding one bit to the current byte and decreasing the despreading m-sequence frequency. This more closely matches the two frequencies which reduces the DC offset. Conversely, if the sample value is less than zero, the comparator output goes high and then the byte 1111 1111 is added to the current byte which is driving the DAC. When the ALU adds 1111 1111, it is the same as subtracting one bit from the current byte and increasing the despreading m-sequence frequency. Once again, this more closely matches the two frequencies and reduces the DC offset.

This design could result in an incorrect adjustment since the lower portion of a positive DC offset waveform could have a negative value and vice versa. As long as the frequency resolution is not too great, the correct adjustment would be made on successive samples and the DC offset would be maintained about the ideal zero reference. The adjustment rate should be sufficient to correct for the fastest frequency change caused by the doppler shift. For example, if the frequency resolution was one hertz per bit and the fastest frequency change was 4 hertz per second, an adjustment rate of

5 samples per second would allow the despreading m-sequence frequency to overtake the spreading m-sequence frequency and slowly oscillate about the zero reference point. However, if the adjustment rate is set too fast the despreading m-sequence will jitter, and acquisition will be lost.

7. Demodulator Synchronization

For the decision making circuitry to provide an optimum result, the integrator in the decision making module must be able to start the integration process as close to the start of an RF pulse as possible and sample the result as near to the end of that same RF pulse as possible. The timing waveforms of Figure 20 relate the demodulator synchronization sequence of events which must take place during each RF pulse period. The subscripted letters relate to the code sequence

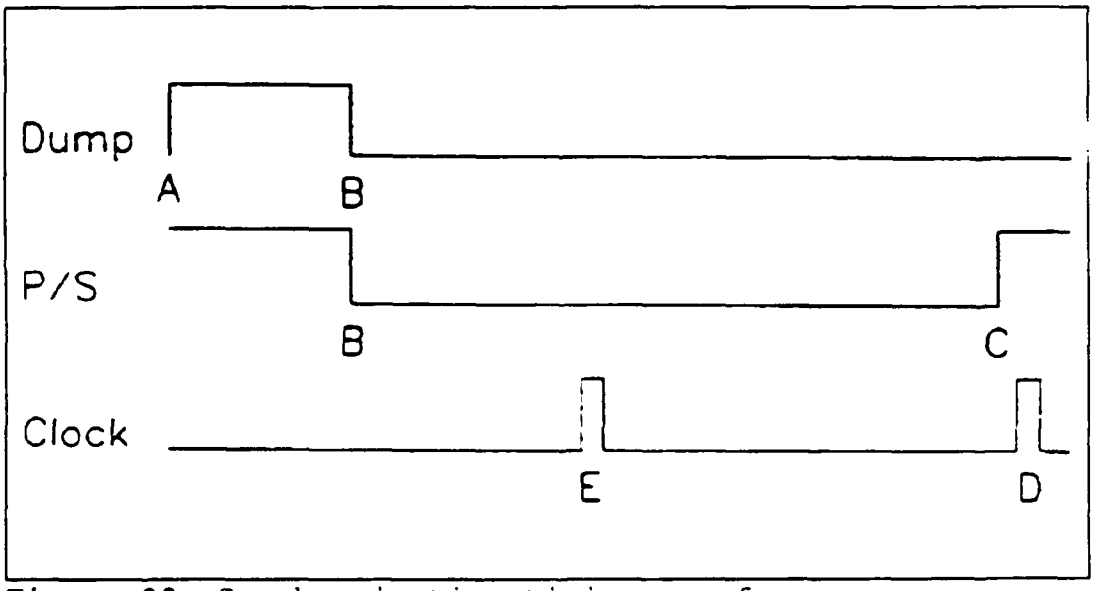


Figure 20. Synchronization timing waveforms

generator groups as discussed later in this section. When the dump timing waveform is high, the RC integrator is connected to ground and all previous capacitor charge and any initial charge due to unreliable signals is removed (transitions between RF pulses must be ignored because of noise introduced during switching). When the dump waveform goes low, the integration process begins and continues until the start of the next RF pulse. At the end of the integration, comparisons are made as to which of the four possible transmitted frequencies contains the greatest signal energy. The result is a parallel load of two bits into the parallel-to-serial converter. This is accomplished by bringing both the P/S waveform and the clock waveforms high. The LSB is immediately available as data out. The MSB is shifted out by the middle clock pulse one-half period later, resulting in data clocked out at twice the rate of the received symbols (two bits) clocked in.

Synchronization is accomplished using knowledge of the m-sequence introduced in section II.A.2. The spreading m-sequence is rewritten in Figure 21 to facilitate the demodulator synchronization discussion. Once the m-sequences are in-phase, it is known that each pulse begins when the code sequence generator (CSG) output is subscripted group A. Subscripted group A initiates the start of the charge dump. Twenty percent of the time into the period, the dump is completed. Integration begins when the CSG output is

subscripted group B. Prior to the end of the integration and in preparation for a parallel load, the parallel-to-serial converter P/S pin is set high when the CSG output is subscripted group C. Three chips before the start of a new symbol and with 80% of the RF pulse period integrated, the symbol with the greatest signal energy is loaded into the parallel-to-serial converter shift register when the CSG code is subscripted group D. The integration process repeats itself, but before the next parallel load, the second bit is shifted to the data output by the clock when the CSG code is subscripted group E, thus completing one cycle.

The circuitry of Drawing A-9 accomplishes all demodulator synchronization. The inverters and 8-input nand gates emit a logical one pulse when their specific CSG code

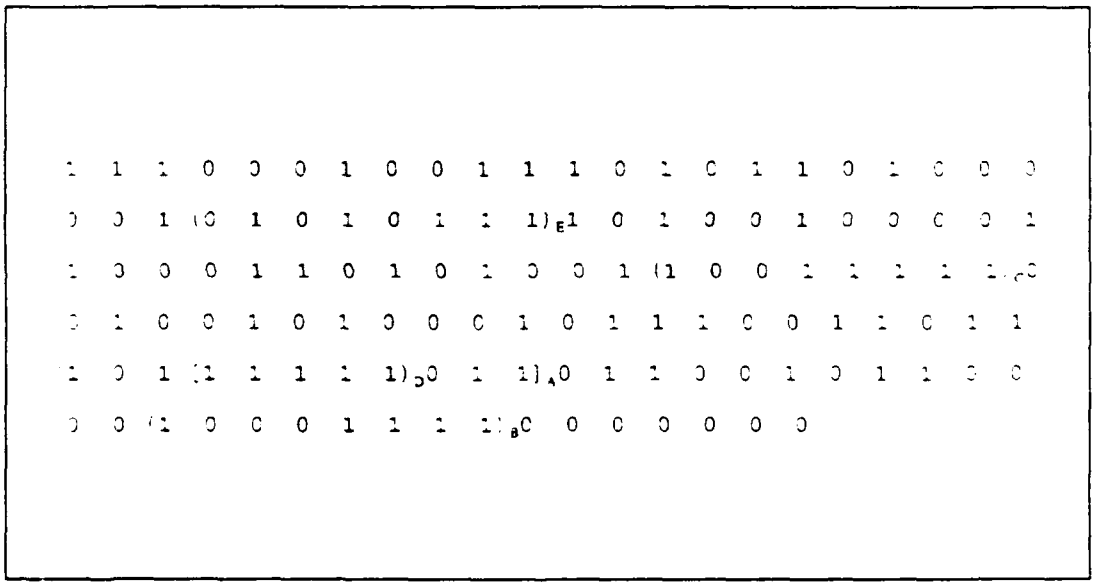


Figure 21. m-sequence, N = 127, taps at stage 3 and 7

bytes are selected. The dump and P/S timing waveforms are achieved by toggling a JK flip-flop. Initiation is not required because the middle clock pulse clears the flip-flops (sets the Q output to zero) on each cycle prior to being toggled high. Because the early minus late feedback voltage maintains a one-half chip phase relationship between the spreading a despreading m-sequences, synchronization can never be further apart than one-half chip. This allows for very accurate synchronization with the modulated data.

III. CIRCUIT CONSTRUCTION

A. 4-FSK SPREAD SPECTRUM MODULATION

1. Serial-to-Parallel Data Conversion Module

The idea to use a shift register and decoder as the basic building blocks for a serial-to-parallel (S/P) converter came from a text on digital logic circuits.[Ref. 1] It was the designer's idea, however, to combine them to form the S/P converter of Drawing A-1. Four analog switches were required to pass the analog frequencies. Switch SW-06 was selected because of its in-house availability and installed per its data sheet. The timing information (set-up and propagation) and pin-out data were found in each components data sheet. For 4-FSK the size of the circuit in Drawing A-1 should be reduced by substituting a 2-4 line latched input decoder for the 4-16 line latched input decoder shown. The latter was used due to availability.

2. Sine Wave Generation Module

The precision sine wave generator design is based on the circuits of [Ref. 2:p. 164] and [Ref. 7:p. 12]. The AD630 (doubly balanced mixer) output at pins 12,13, and 14 is a 1.8V peak-to-peak square wave which is fed into an integrator via resistor R1. The integrator output at pin 6 of the LM318 operational amplifier is a 1.8V peak-to-peak triangular wave

which is fed into pin 1 of the AD639 (trigonometric function generator). The AD639 output at pins 13 and 14 is a sinusoid whose frequency and accuracy are based on the frequency and accuracy of the triangular wave input at pin 1. "The AD639 can generate continuous sinewaves of very low distortion using a linear, highly symmetric triangle wave of ±1.8 V amplitude." [Ref. 7:p. 6] To produce a precision sine wave, build the sine wave generator of Drawing A-2, replace resistor R1 with a 10kΩ variable resistor and adjust until the triangle wave output of the integrator equals the required frequency, replace resistor R2 with a 5kΩ variable resistor and adjust until the sine wave output of the AD639 has minimum distortion as viewed on an oscilloscope and/or a spectrum analyzer, and finally replace the variable resistors with fixed-value resistors.

The LM318 operational amplifiers in the low pass filters and buffers of Drawing A-2 must have their power supplies capacitively bypassed and be decompensated for stability as shown in Drawing B-3 and Drawing C-1.

3. Spread Spectrum Module

The digital logic m-sequence generator of Drawing A-3 consisting of the shift register, exclusive-or, and inverter was constructed from knowledge of the generator polynomial and the SSRG of Figure 7. This circuit also matches the 7 stage m-sequence of [Ref. 8:p. 21-12]. The comparator circuit was taken from [Ref. 9:p. 2-54]. The variable resistors used in

adjusting the comparator power supply voltages (and hence the upper and lower values of the comparator output) must be 10 or 25 turn potentiometers to allow for adequate resolution to fine-tune the values of plus and minus one volt output at pin 1. The one volt magnitude is not critical but the magnitudes of the upper and lower output being equal is important. Set the reference variable resistor connected to pin 2 to approximately 2.5 volts. The doubly balanced mixer (DBM) circuit was taken from [Ref. 10:p. 7]. For best results, minimize the offset voltage in accordance with the procedure on offset voltage nulling. [Ref. 10:p. 6]. Construct the buffer as discussed in Appendix C.

B. 4-FSK SPREAD SPECTRUM DEMODULATION

1. Fourth Order Band Pass Filter Module

All of the LM318 operational amplifiers on the circuit diagram of Drawing A-4 do not show bypass capacitors on the power supplies or decompensation capacitors. These were left off so that a cleaner, more concise diagram could be presented. These must be included as shown on the band pass filter of Drawing B-2 or as shown on the buffer of Drawing C-1. Place all bypass capacitors as close to the power supplies as practical. The high frequency section of the circuit is located between the input to the band pass filter and the output of the buffer. In this region keep all leads as short as possible.

The band pass filters were taken from [Ref. 11:pp. 18-22] with the choice of operational amplifiers made by the designer for their wide small signal bandwidth and high slew rate. If operational amplifiers with a different small signal bandwidth than the LM318 (small signal bandwidth equals 15 MHz) are used, then the values of the passive elements must be recalculated using the procedure provided in Appendix B.

2. Decision Making Module

Construct the DBM as shown in Drawing A-5 and adjust the variable resistors according to section III.A.3. to minimize the offset voltage. Install capacitors on the operational amplifiers as indicated on the buffer of Drawing C-1. The non-inverting amplifiers, envelope detectors, low pass filters, integrators, and comparators were designed using guidance and/or sample circuits from [Ref. 2:p. 57], [Ref. 5:p. 273], [Ref. 12:pp. 37-39], [Ref. 13:pp. 233-234], and [Ref. 9:p. 2-54] respectively. The digital logic required to make the comparisons and the implementation using inverters, three input nand gates, an encoder, and decoder were the designer's ideas. All pin positions were taken from each component's data sheet.

3. Frequency Sweep Module

All components in this module were constructed from each component's data sheet. The DAC and VCO data sheets include these application circuits with notes. The VCO output

is a 0V to -15V square wave. Efforts to modify the circuit to output a positive square wave were unsuccessful. The use of a comparator was successful in creating a 0V to +5V square wave to clock the despreading m-sequence. Using an oscilloscope, adjust the 500 Ω variable resistor between VCO pins 4 and 6 to balance the square wave duty cycle. Set the comparator reference voltage at pin 3 to -7.5V and adjust the variable resistor connected to pins 7 and 8 until the comparator square wave output alternates between 0V and +5V.

4. Early Minus Late Module

The early/late m-sequence generator uses the same components and construction guidance found in paragraph III.A.3. used to build the modulator spread spectrum module with the exception of the additional shift register. The additional shift register was the designer's idea for one method of producing an incrementally advanced and delayed version of the punctual m-sequence. It was determined through experimentation that for the circuit of Drawing A-7, a clock rate of 4 kHz into the sampling switch produced useable early and late ACF signals through the band pass filters. The 10 kΩ variable resistors which are summed into the pair of inverting adders must be adjusted to remove the DC offset. This should be done while the two m-sequences are sliding past one another (before any feedback is sent to the frequency sweep or track modules). Not shown on the final inverting adder is the 10 kΩ

variable resistor connected between pins 1 and 5 to remove the operational amplifiers DC offset. With zero volts connected to all summing inputs, adjust the variable resistor until the output at pin 6 is 0V. Adjust the 100 kΩ variable resistor at the operational amplifier output, pin 6, until the feedback voltage is 40 mV peak-to-peak. After the m-sequences lock together, increase the feedback voltage until the despreading m-sequence starts to jitter then reduce the voltage until the jitter stops. Adjust the comparator variable resistors to ±2V. It is important that these reference voltages be greater than the maximum noise level and less than the correlated early and late minimum voltages (inputs to comparator pins 2 and 3 respectively).

5. Track

The or gates were included as a buffer between the analog comparator and the digital latch. There are no adjustments required in this module.

6. Demodulator Synchronization

The eight input nand gates available to the designer did not have a non-inverting (and) output as shown in Drawing A-9; therefore, the inverters at the nand output were required to produce the desired eight input nand gate. The JK flip-flops were designed to toggle using the data sheet truth table. There are no adjustments required in this module.

IV. EXPERIMENTAL RESULTS

A. 4-FSK SPREAD SPECTRUM MODULATION

1. General

Unless otherwise advised all of the figures in the experimental results chapter were plotted using a Hewlett-Packard 54510A Digitizing Oscilloscope with Think Jet Printer. Axis scales have been left out but were included in the captions in time per division and volts per division respectively.

2. Serial-to-Parallel Data Conversion and Precision Sine Wave Generator Module

The serial-to-parallel (S/P) converter was first tested manually by clocking the four possible data combinations of zeros and ones into the data input and then verifying that the correct frequency was output to the spread spectrum module. The bit pairs of 00, 10, 01, and 11 correctly produced the output frequencies of 76.2, 152.4, 228.6, and 304.8 kHz respectively. A maximal-length sequence generator of 15 chips was built to supply a repetitive, continuous string of data for follow-on tests. In Figure 22, the bottom waveform is the digital m-sequence (length of 15). One entire sequence and part of a second is shown. The top waveform is the output from the S/P converter module. After each pair of bits is

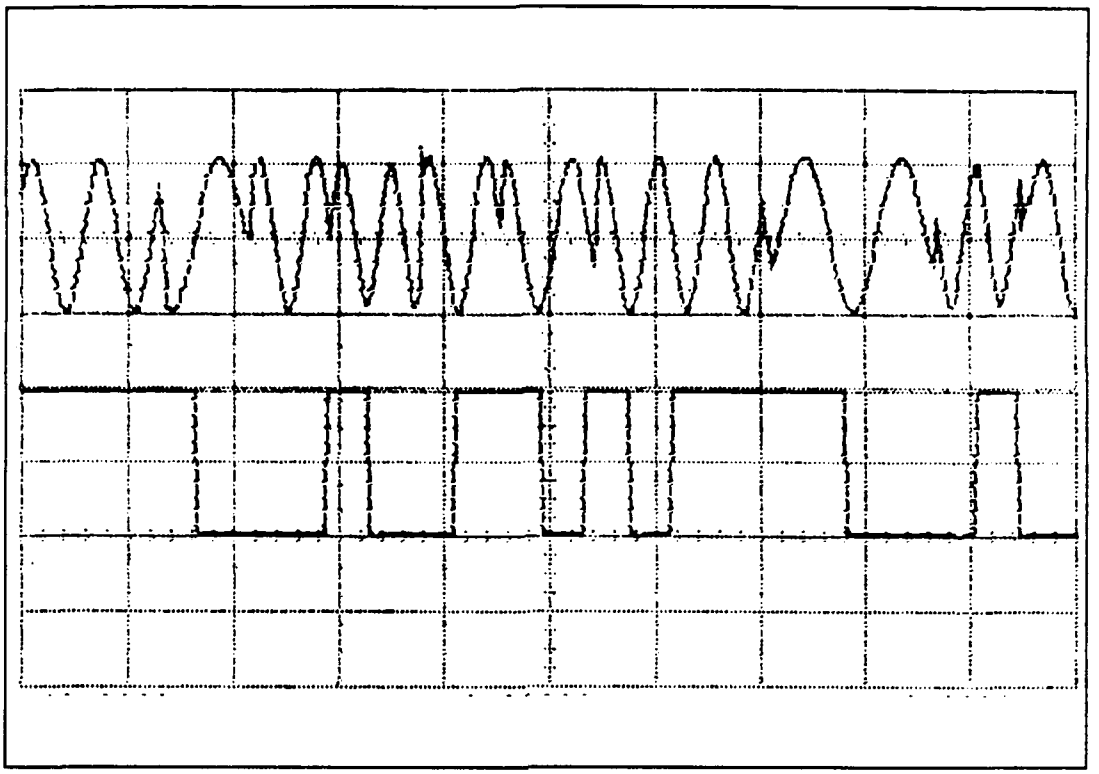


Figure 22. Bottom: Data in, 2.0ms, 1V; Top: Frequencies out, 2.0ms, 1V

grouped together, the decoder selects the appropriate switch and outputs the appropriate frequency. Notice the phase changes which signal the start of the next RF pulse. This was expected since the S/P converter was designed to be discontinuous-phase FSK (see Figure 3).

3. Spread Spectrum Module

The bottom waveform of Figure 23 is a portion of a 76.2kHz RF pulse prior to being mixed with the spreading m-sequence (input to the DBM). The top waveform is the same portion only after being mixed with the m-sequence. For each 180 degree phase change in the m-sequence, a corresponding 180

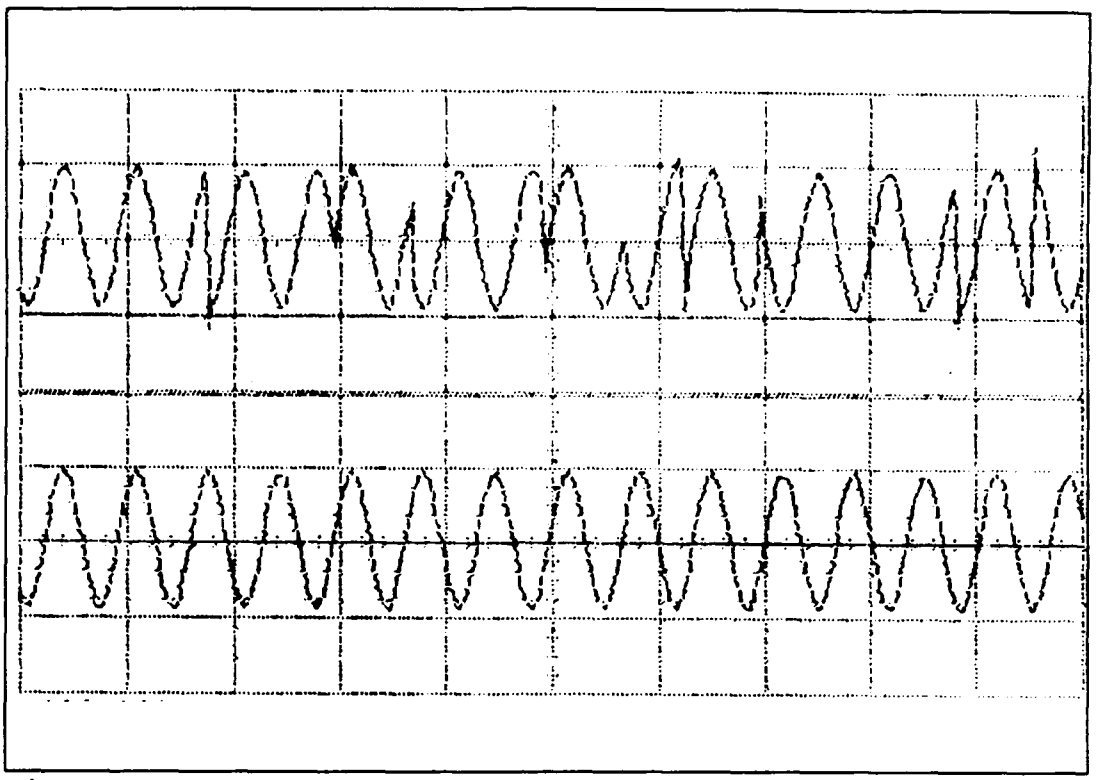


Figure 23. Bottom: RF pulse prior to be mixed with the spreading m-sequence, 20.0μs, 1V; Top: RF pulse after being mixed, 20.0μs, 1V

degree phase change takes place in the signal. As discussed in section A.3., the shortened RF pulse period causes the signal bandwidth to increase. Figures 24 and 25 show the 1200 bit per second, 4-FSK, signal spectral density before and after being spread by the m-sequence (as seen on a Hewlett Packard 8567A Spectrum Analyzer). As expected the bandwidth has widened and the amplitude decreased. It was difficult to measure the spread spectrum bandwidth due to the proximity of the 4-FSK signals.

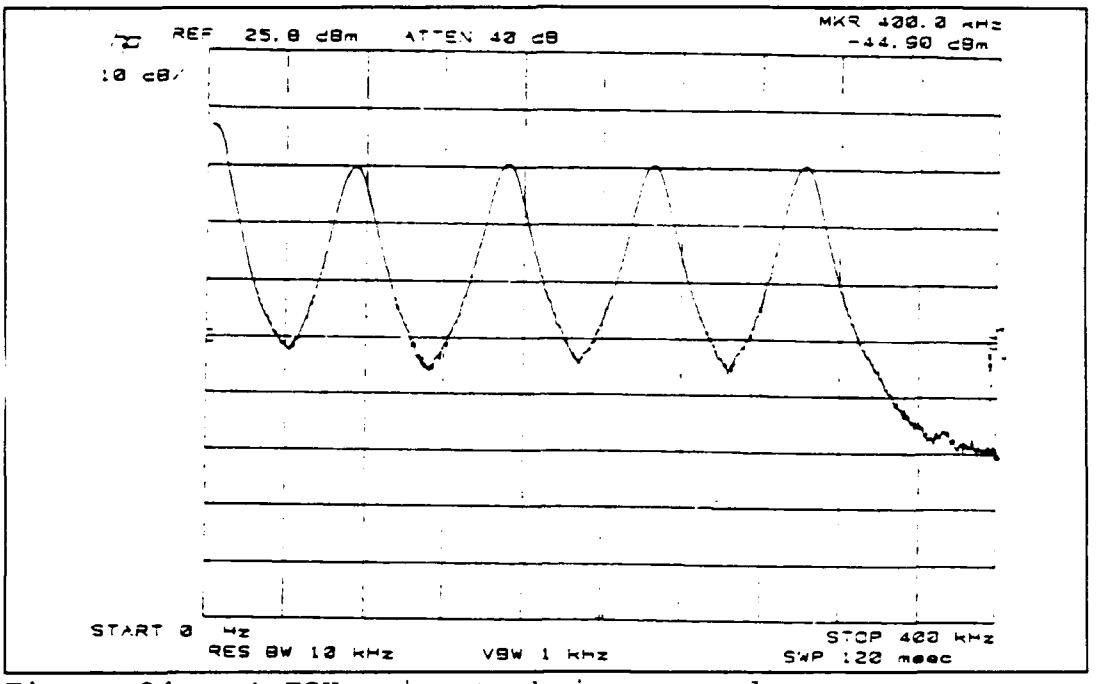


Figure 24. 4-FSK prior to being spread

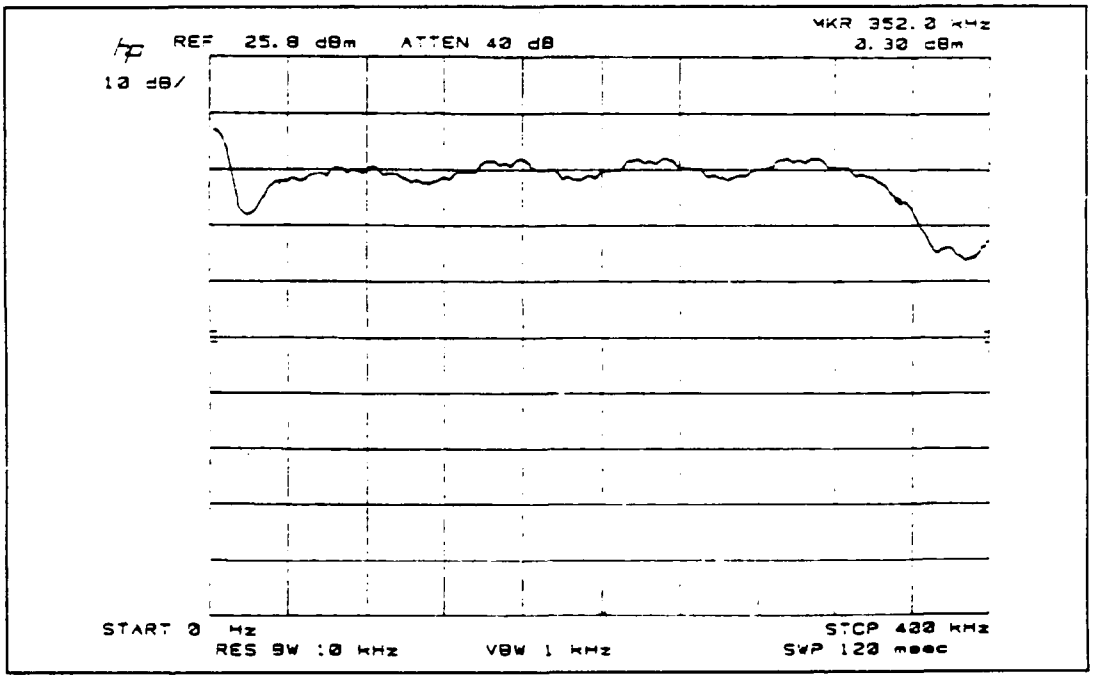


Figure 25. 4-FSK after being spread

B. 4-FSK SPREAD SPECTRUM DEMODULATION

1. General

Testing was accomplished only after the demodulator was independently able to acquire and track the 4-FSK, spread spectrum, modulated signal. All figures with correlated waveforms are a result of this acquisition and track. The only connection between the modulator and demodulator is the channel (hard wired).

2. Band Pass Filter Module

Three of the band pass filters performed as designed. The band pass filter which was designed to have a center frequency of 228.6 kHz was actually centered at approximately 250 kHz. This filter was redesigned with passive elements which moved the center frequency down to the desired location.

3. Decision Making Module

From the input to the band pass filters to the output of the integrator amplifiers, there are four similar circuits. To reduce the number of repetitive statements and shorten the explanation of this module, a portion of a single RF pulse will be followed through the top branch in Drawing A-5. The bottom waveform of Figure 26 is the received spread spectrum signal from the modulator. After being mixed with the uncorrelated m-sequence, additional phase changes are added by the despreading m-sequence (top waveform) causing the bandwidth to be further increased. The waveform at the bottom

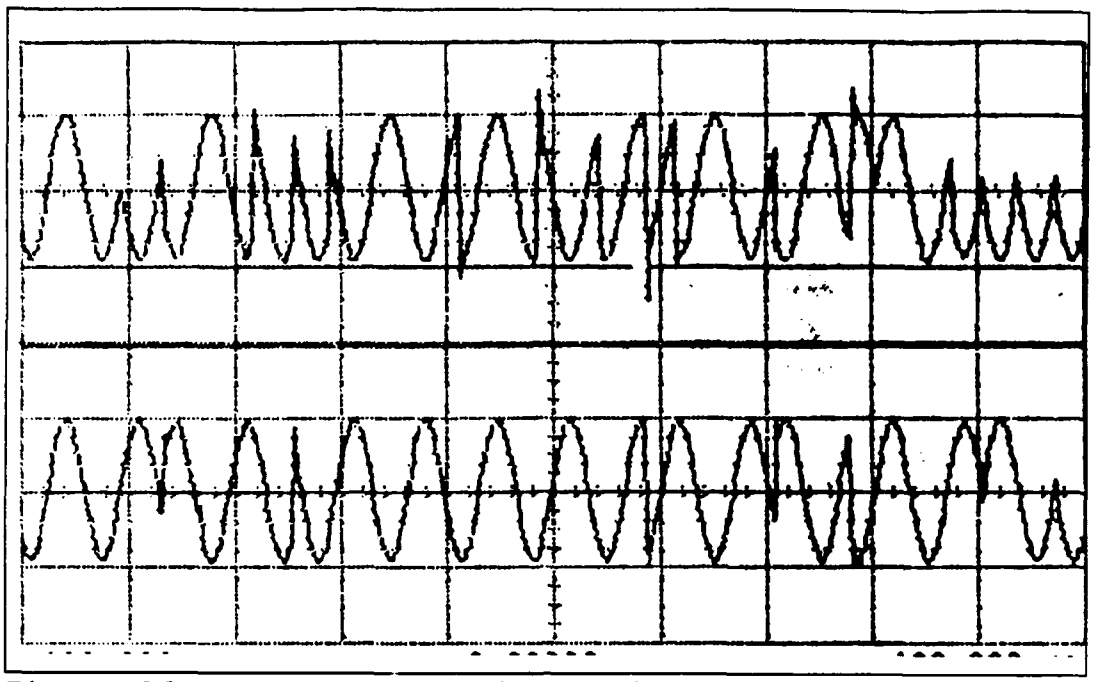


Figure 26. Bottom: Received signal, 20μs, 1V; Top: Uncorrelated received signal, 20μs, 1V

of Figure 27 is again the received signal only now the top waveform is of the correlated signal. For each phase change in the received signal, there is now a second phase change to cancel the first. Notice that the second phase change cancellation does not occur at the same position as the first. This is a result of the m-sequences being slightly out of phase. This is to be expected since the m-sequences will oscillate about the zero phase point. For a final comparison in Figure 28, the bottom waveform is the RF pulse prior to being spread by the modulator, and the top waveform is the RF pulse after the demodulator despreads the received spread spectrum signal. As can be seen in Figure 28, spreading and despreading are inverse operations. Because the operations

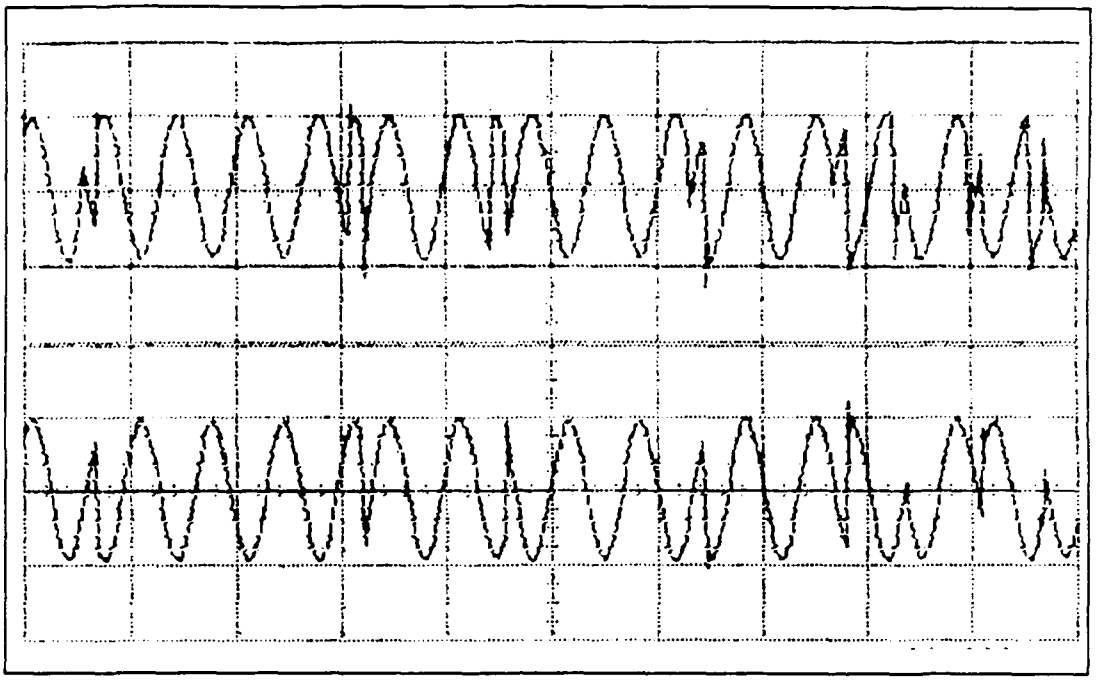


Figure 27. Bottom: Received signal, 20μs, 1V; Top: Correlated received signal, 20μs, 1V

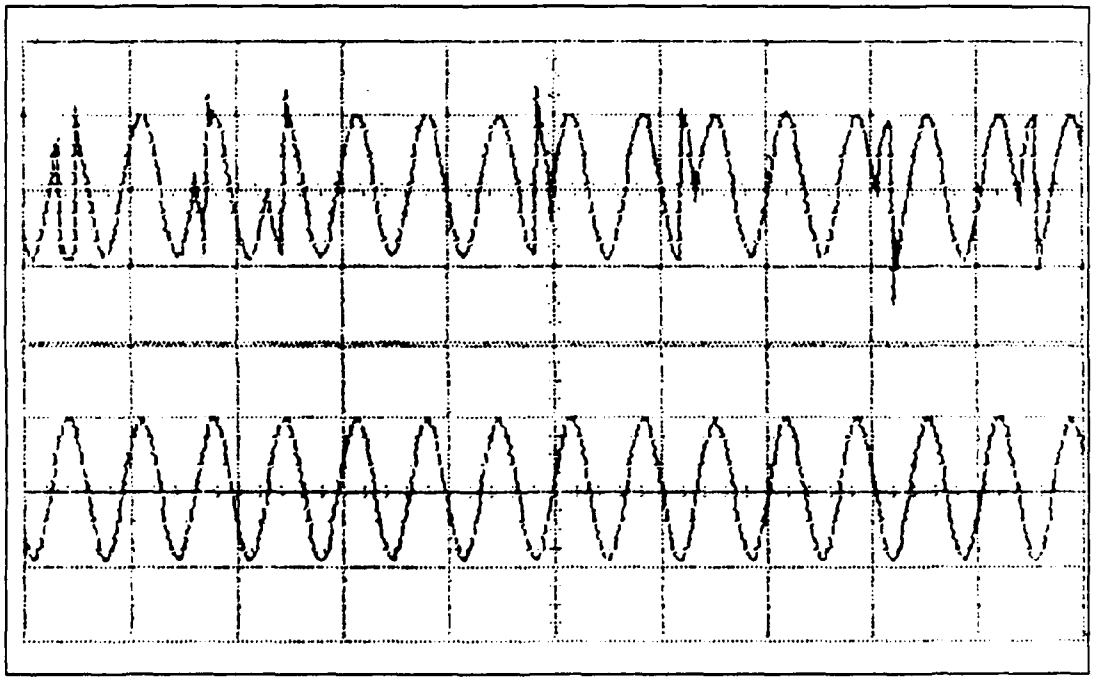


Figure 28. Bottom: RF pulse prior to being spread, 20μs, 1V; Top: RF pulse after being despread, 20μs, 1V

occur at the output of the demodulator and the input of the demodulator, the operations are transparent to the rest of the circuit. The bottom waveform of Figure 29 is the uncorrelated input to the bank of band pass filters. From the top waveform, the magnitude of the uncorrelated RF pulse is no longer constant but varies pseudorandomly as the m-sequences move in and out of phase. By contrast in Figure 30 the output

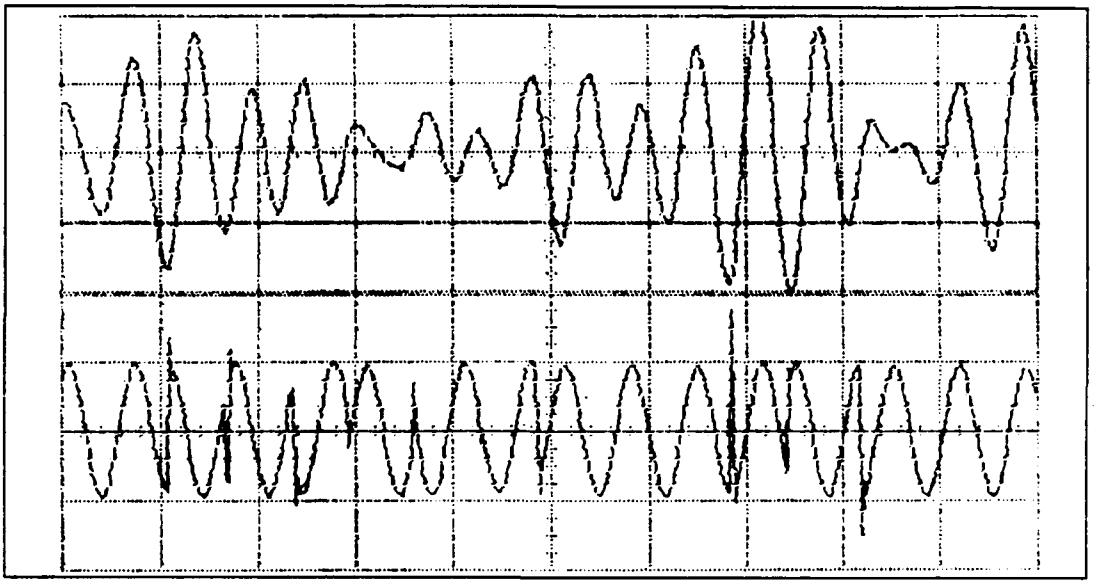


Figure 29. Bottom: Uncorrelated input to BPF, 20μs, 1V; Top: Uncorrelated output from BPF, 20μs, 1V

magnitude of the band pass filter (top waveform) is nearly constant for the correlated input (bottom waveform). Figures 31 and 32 show a comparison between the uncorrelated and correlated RF pulses and its effect on the envelope detector's low pass filter output (bottom waveform) and the integrator amplifier output (top waveform). Since the integrator output voltage level is ultimately used to determine the received

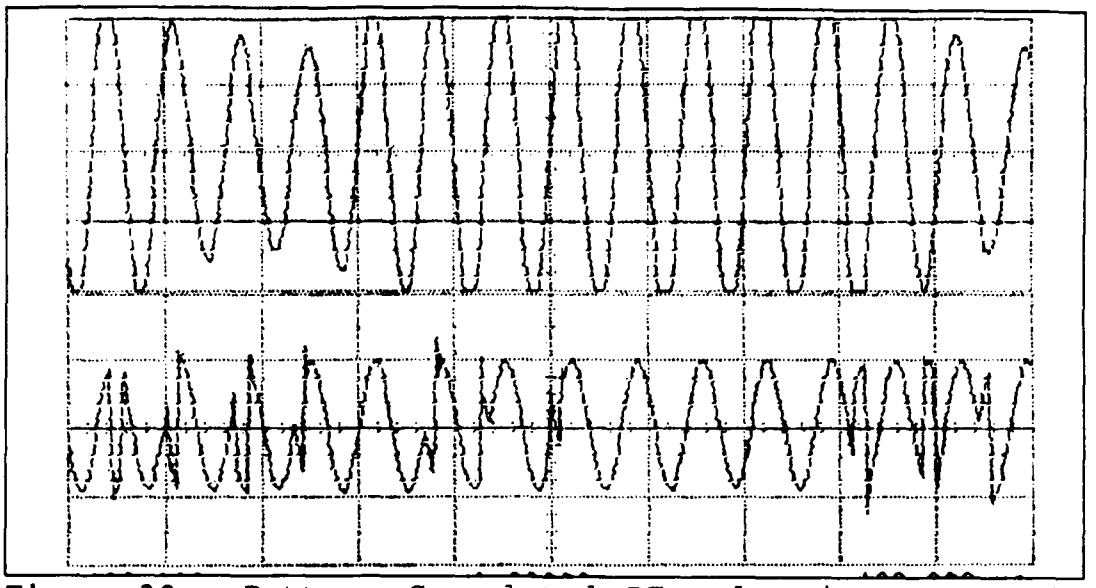


Figure 30. Bottom: Correlated RF pulse input to BPF, 20μs, 1V; Top: Correlated RF pulse out of BPF, 20μs, 1V

data, a highly correlated signal increases the signal-to-noise ratio and reduces the bit error rate. To verify that the comparators and digital logic integrated circuit chips were properly connected and the synchronization timing (to be discussed later) was properly calculated, the 15 chip m-sequence was clocked as data into the modulator (Figure 33, top waveform) and compared with the data clocked out of the demodulator (Figure 33, bottom waveform). From this figure the received data is a delayed duplicate of the transmitted data.

4. Frequency Sweep Module

Because eight bit digital components were used to construct the sweep module, the frequency sweep range was limited by the frequency resolution. A frequency resolution

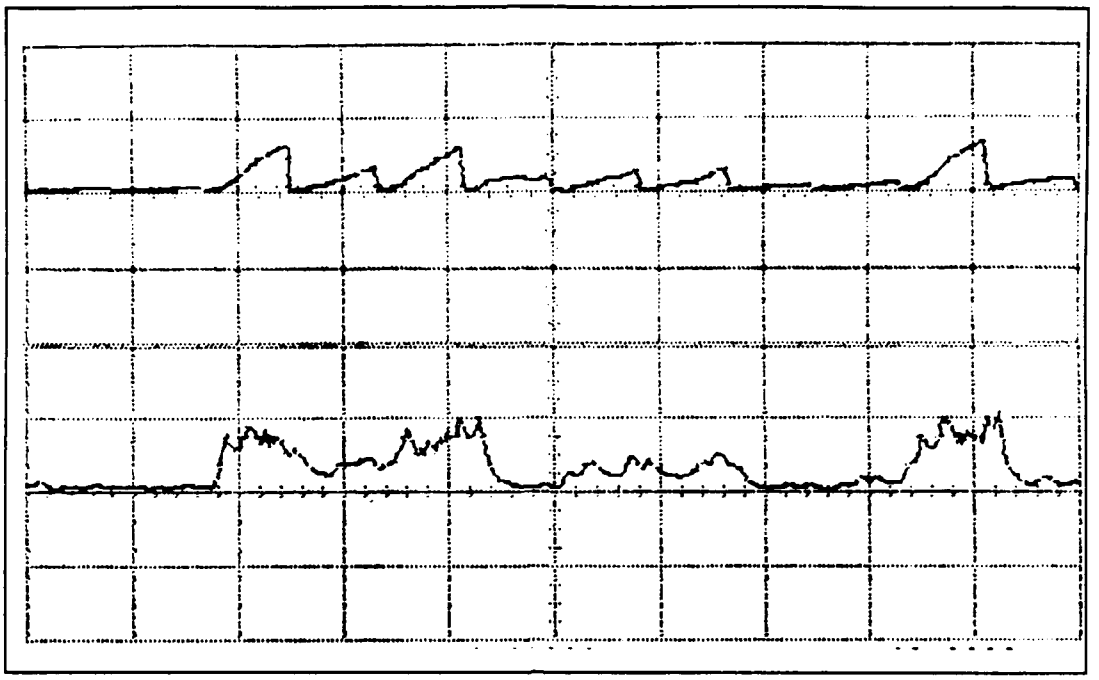


Figure 31. Bottom: Uncorrelated envelope detector output, 2.0ms, 2V; Top: Uncorrelated integrator output, 2.0ms, 4V

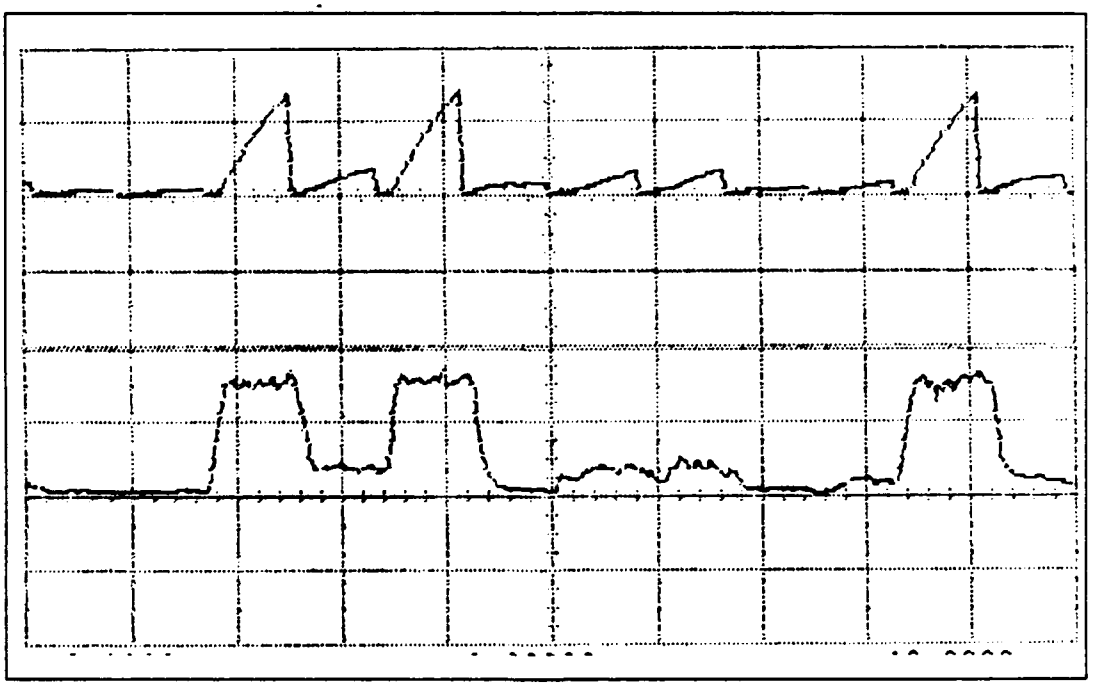


Figure 32. Bottom: Correlated envelope detector output, 2.0ms, 2v; Top: Correlated integrator output, 2.0ms, 4V

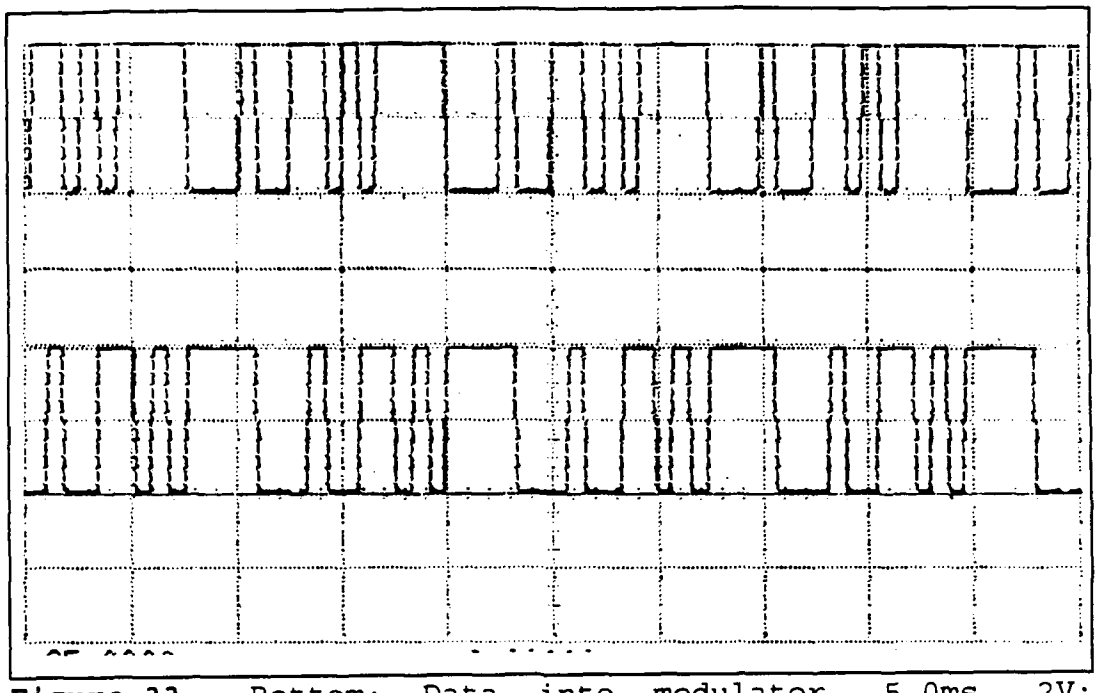


Figure 33. Bottom: Data into modulator, 5.0ms, 2V; Top:Data out of demodulator, 5.0ms, 2V

of six hertz per bit worked well for this design. A coarser resolution resulted in increments too great for the demodulator to maintain track after acquisition. With these constraints the sweep range was approximately 1.5 kHz. Using the variable resistor in the DAC block of Drawing A-6, the sweep range was centered about the modulator chip rate of 76.2 kHz. In addition to sweeping the range of possible m-sequence frequencies, the frequency sweep module accepts analog voltage feedback into the 10kΩ resistor in the DAC block and digital voltage feedback into the latch in the digital count block.

5. Early Minus Late Module

Figures 34 and 35 are the one-half chip early (top) and one-half chip late (bottom) waveforms represented using single and dual axis displays. The inverted late correlation waveform was produced by inverting the diode in Drawing A-7. Summing the early and inverted late correlation waveforms resulted in the early minus late waveform of Figure 36. This is the analog feedback control voltage which holds the m-sequences within one-half chip in-phase. The waveforms of Figures 34 through 36 are only generated when the two m-sequences are sliding past one another. When the m-sequences lock together, the early and late waveforms ramp up and

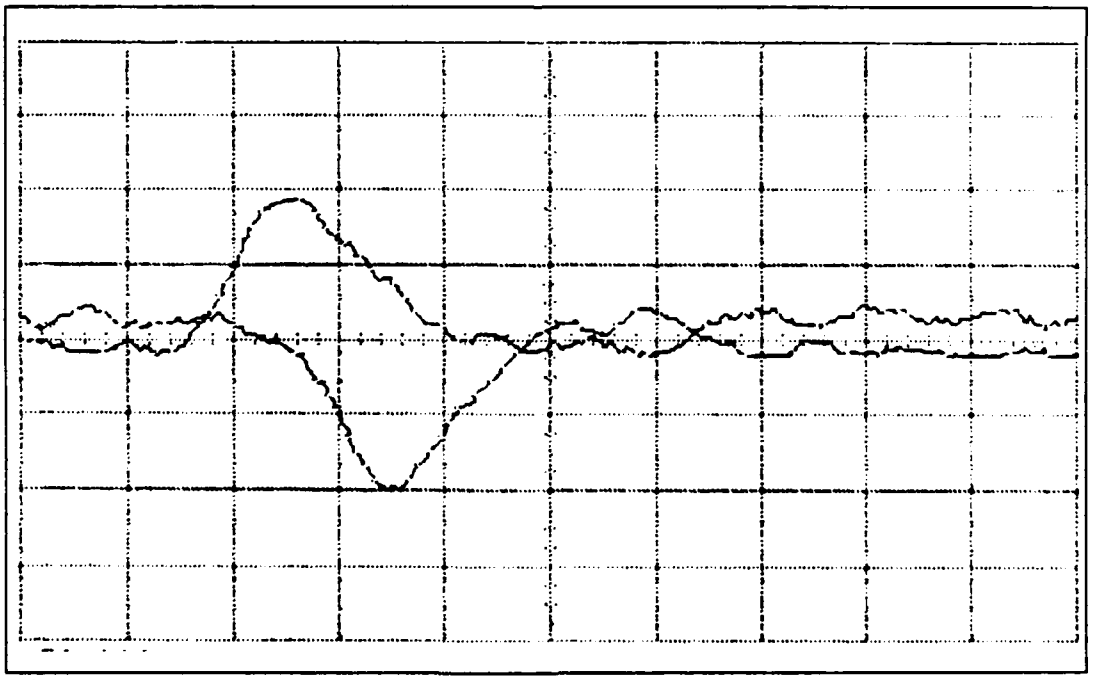


Figure 34. Bottom: Late ACF, 10.0ms, 5V; Top: Early ACF, 10.0ms, 5V

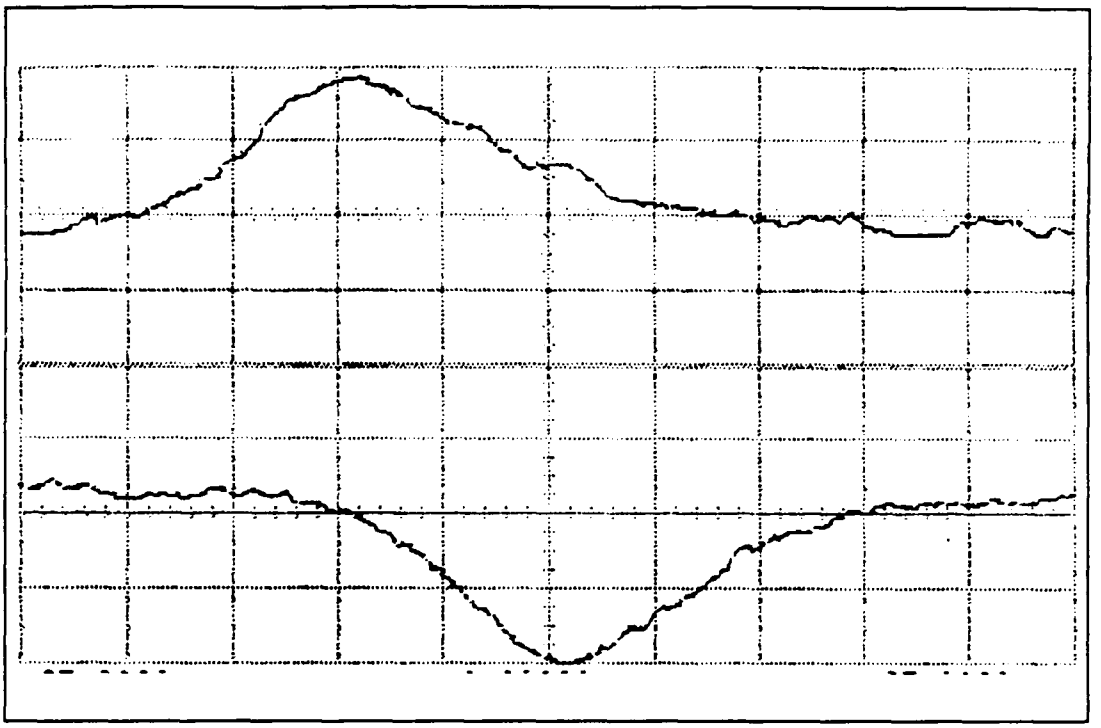


Figure 35. Bottom: Late ACF, 5.0ms, 5V; Top: Early ACF, 5.0ms, 5V

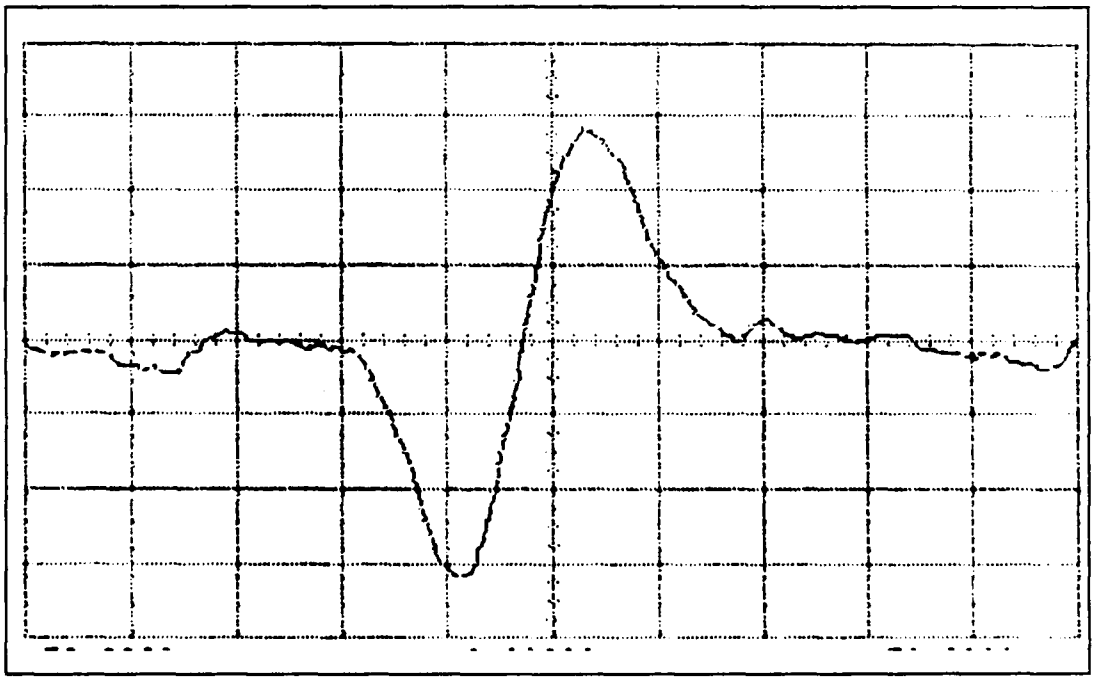


Figure 36. Early ACF minus late ACF, 10.0ms, 2.5V

oscillate about their mid-range voltages (See Figure 37). The early minus late waveform oscillates about a reference voltage (DC offset) determined by how close the two m-sequence frequencies were together at acquisition. If the m-sequences' phase line-up just as the frequencies matched, then the DC offset would be zero (See Figure 38). Since this is the exception rather than the rule, some DC offset exist (See Figure 39). This occurrence will be used to track a doppler shift.

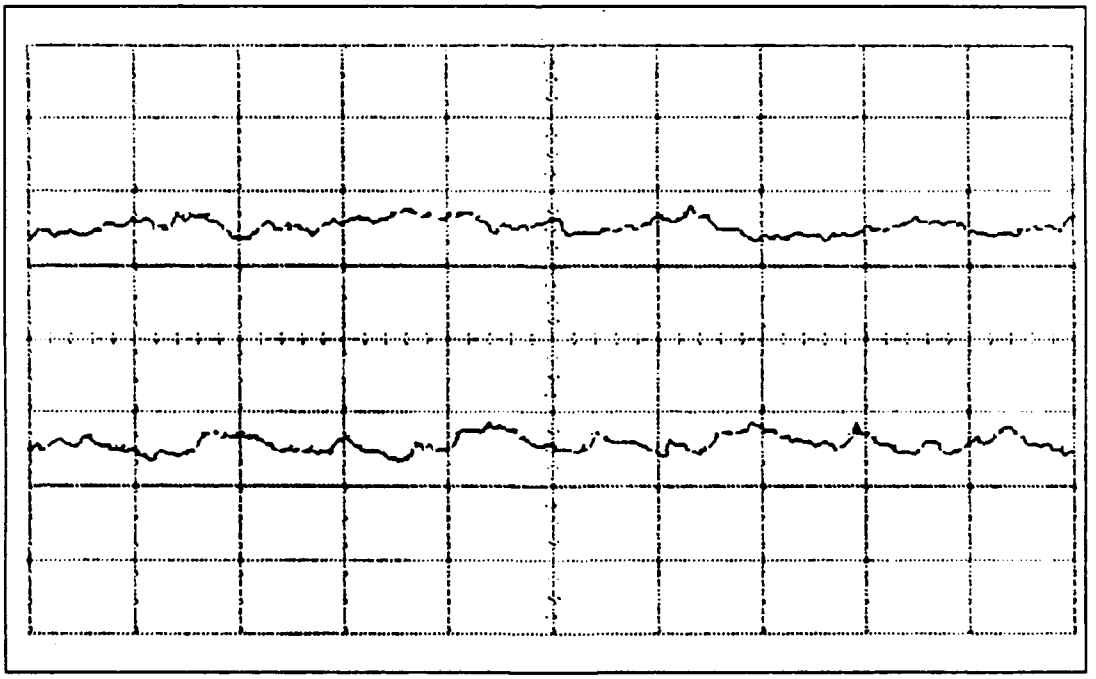


Figure 37. Bottom: Late ACF, 10.0ms, 5V; Top: Early ACF, 10.0ms, 5V

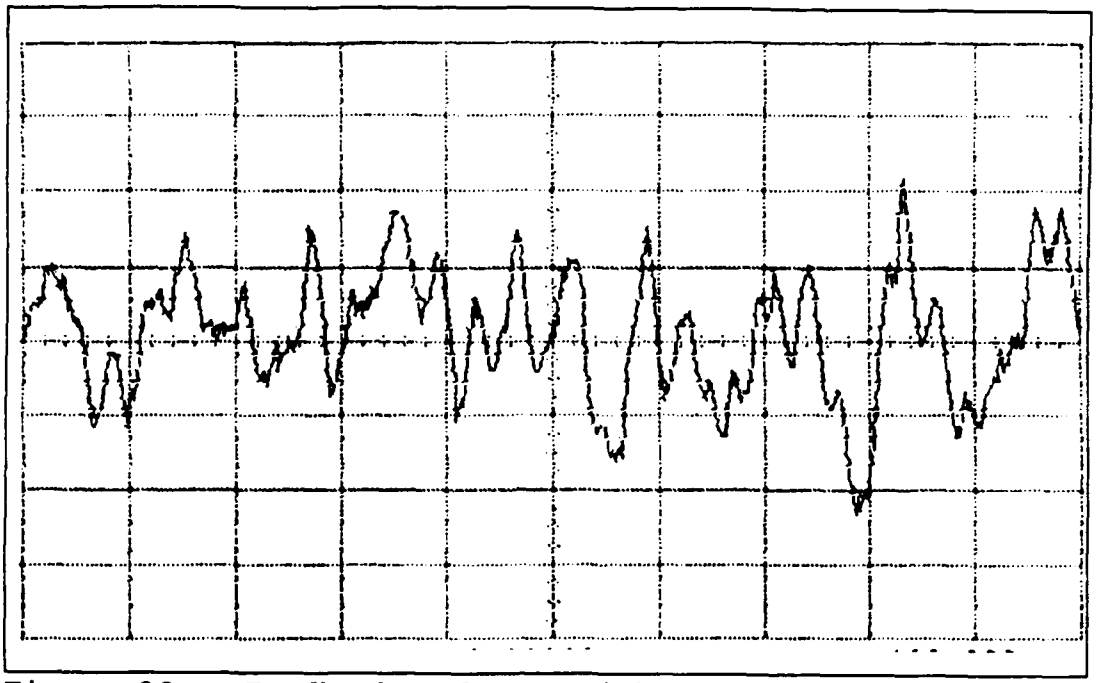


Figure 38. Feedback voltage without DC offset, 20.0ms, 500mV

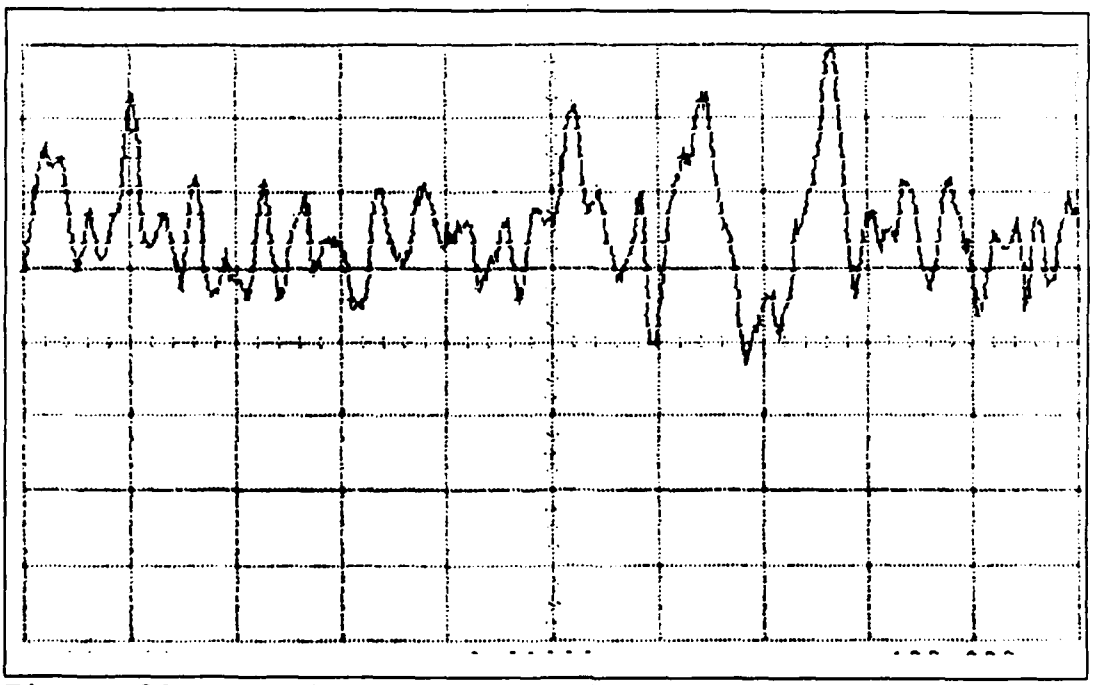


Figure 39. Feedback voltage with DC offset, 20.0ms, 500V

6. Track

The track module of Drawing A-8 monitors the early minus late waveform DC offset and adds or subtracts one bit at a rate of 30 times per second. With a frequency resolution of 6 hertz per bit, a doppler shift of less than 180 hertz per second can be tracked. To test this circuit, a second frequency sweep module was constructed, except the digital count and DAC were replaced with a 0.44 pF polypropylene capacitor and a FET unity gain buffer. The capacitor was charged to a voltage slightly higher than the voltage required to drive the VCO at the upper range frequency. When the voltage source was removed from the capacitor, the capacitor would discharge current at a rate equal to the FET input bias current (50pA). The voltage would decrease at a linear rate equal to the rate corresponding to the max doppler shift of six hertz per second. The demodulator successfully tracked a six hertz per second doppler shift over its full range of frequency sweep (1.5 kHz).

7. Demodulator Synchronization

Let the synchronization timing cycle begin at the start of an RF pulse. Recall from section II.B.7. that the integrator charge would be dumped at the start of each RF pulse. From Figure 40, the 275 us pulse (the longest pulse, second from left) closes all four switches in Drawing A-5 to

ground which dumps (discharges) all four integrators. When the dump pulse goes low, integration begins and continues until the next dump pulse (partially drawn at the far right of Figure 40). Prior to selecting the RF pulse with the greatest energy, the parallel-to-serial (P/S) converter must be set up for a parallel load from the encoder. This is accomplished by the 215 us P/S pulse (the longest, first from left) in Figure 41. While P/S pulse is high, the parallel mode is selected and the clock pulse (centered in the parallel load pulse of Figure 41) activates the parallel load. This also moves the first bit of the encoded pair out of the serial-to-parallel converter. This is the same clock pulse as can be seen

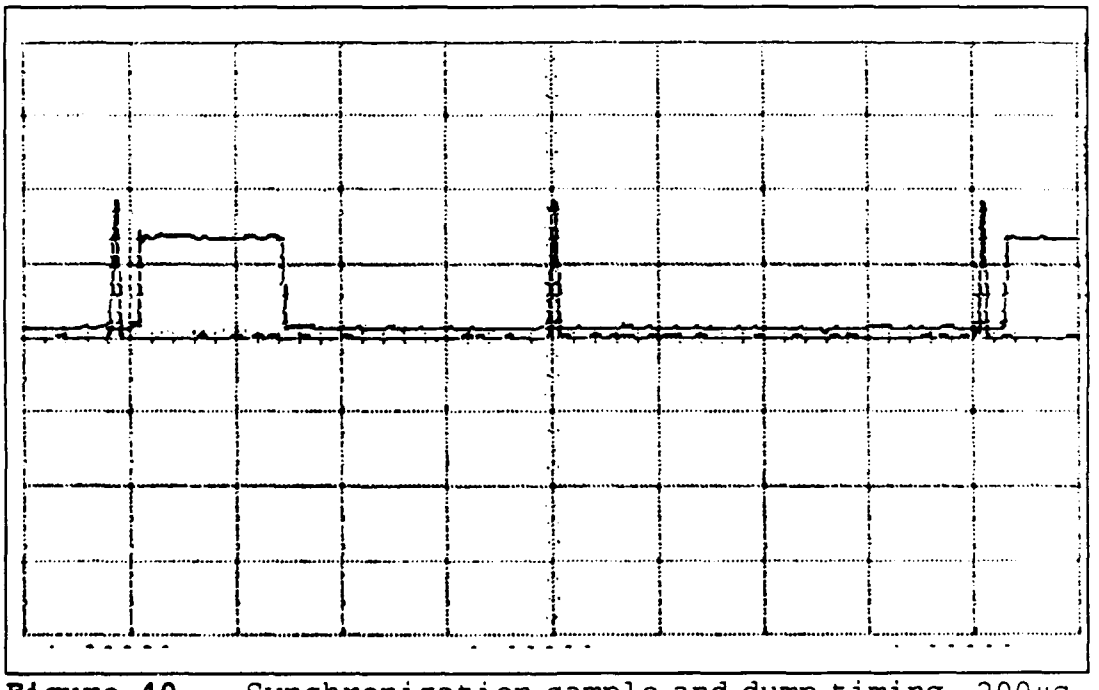


Figure 40. Synchronization sample and dump timing, 200μs, 2.5V

occurring right before the start of an integrator dump (end of RF pulse) in Figure 40. When the P/S pulse goes low, the serial mode is activated. The next clock pulse (not centered in the P/S pulse of Figure 41) moves the second of the two encoded bits out of the parallel-to-serial converter. This cycle repeats itself with the start of the integrator dump.

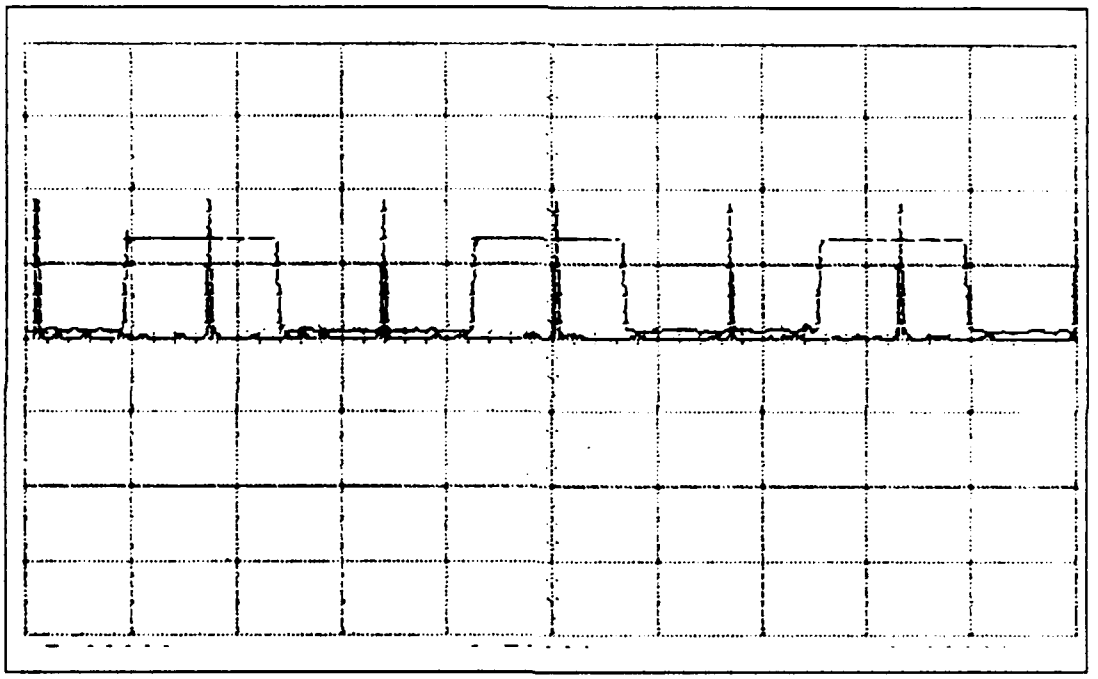


Figure 41. Synchronization parallel load timing, 500μs, 2.5V

8. Probability of Bit Error

Probability of bit error testing was accomplished using the following equation taken from [Ref. 4:p. 44]:

$$(S/N)_{dB} = 20\log_{10}\left(\frac{V_{rms\ signal}}{V_{rms\ noise}}\right)$$

The modulator signal was a 1V amplitude RF pulse. For sinusoidal waveforms $V_{rms} = V/\sqrt{2}$; therefore, $V_{rms\ signal} = 1/\sqrt{2}$. $V_{rms\ noise}$ was generated by a Wavetek, model 132, VCG/Noise Generator with a sequence length of 2^{20}-1 and a noise frequency of 160 kHz to 1.6 MHz. The $V_{rms\ noise}$ amplitude was determined by measuring the value read on an averaging AC voltmeter (Hewlett-Packard 427A Voltmeter) and multiplying that value by 1.13.[Ref. 12:p. 454] The noise was added to the output of the modulator using a summing amplifier. A test circuit was designed and built. It took the modulator input data and compared it with the demodulator output data using an exclusive-or gate (XOR). When the inputs to the XOR disagreed the XOR output went high. In the middle of each bit period, the output of the XOR was clocked into a 4-bit shift register. If the shift register output (Q1) goes high, the positive-going pulse clocks a counter and one error is recorded. At the start of each bit period, the shift register is cleared which prepares it to clock the next error. LEDs were connected to the counter output via a driver so that errors could be

visually counted. Two sets of data were recorded, one with an analog feedback rate of 5 Hz and a second with an analog feedback rate of 10 Hz. The results are plotted in Figure 42. Based on these limited tests, a SNR greater than -1.25 dB would be required to have a bit error rate less than 10^{-5}.

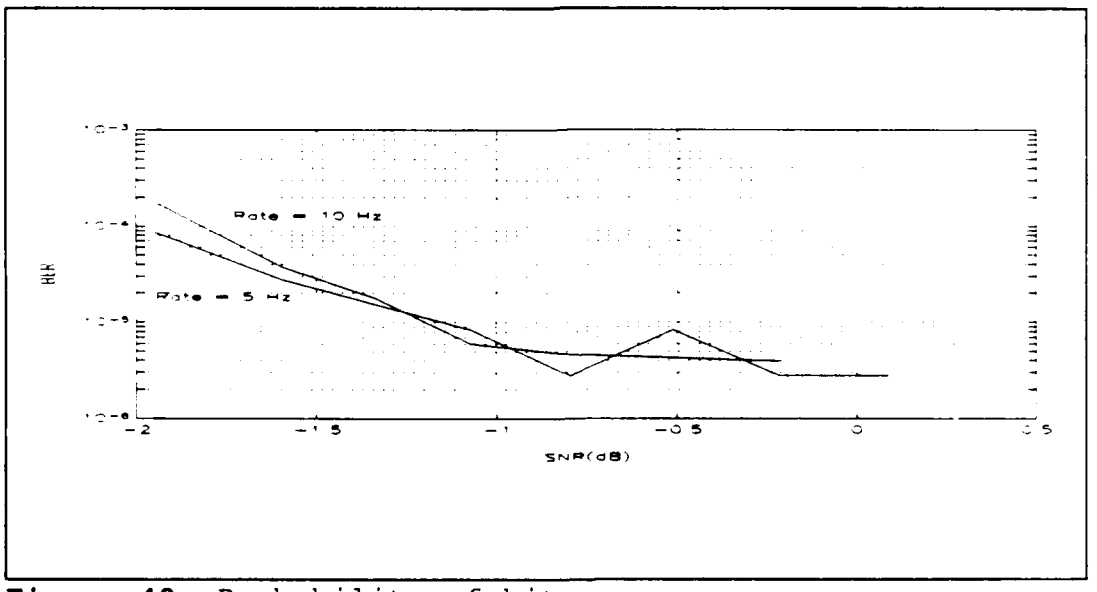


Figure 42. Probability of bit error

V. RECOMMENDED DESIGN MODIFICATIONS

A. 4-FSK SPREAD SPECTRUM MODULATION

Reduce the size of the S/P convertor module by replacing the 4-16 line latched input decoder with a 2-4 line latched input decoder. No change in performance would result. For greater stability replace the sine wave generators (the AD630, AD639, and LM318 integrator) with crystal oscillators. The sine wave generators were initially selected because they could be adjusted over a wide range of frequencies which allowed for design changes. The crystal oscillators take longer to receive and allow for only slight frequency adjustment. The second order low pass filters could be changed to fourth order by cascading a second identical stage. This would further reduce the signal energy in the lower frequencies' harmonics from showing up as noise in the demodulator's higher frequencies envelope detectors.

B. 4-FSK SPREAD SPECTRUM DEMODULATION

In the frequency sweep module, replace the 8-bit counter, latch, and digital-to-analog convertor with at least 12-bit components to greatly increase the frequency range and retain adequate resolution of the frequency sweep module. 12-bit components would allow for 4,096 frequency steps vice the 256 frequency steps available with 8 bit components. Increased

number of frequency steps results in a frequency resolution of 4.9 hertz per bit over a 20 kHz doppler shift. It was demonstrated on the prototype that the maximum doppler shift could be tracked over a limited range of frequencies. 12-bit components would be capable of tracking through the full frequency range.

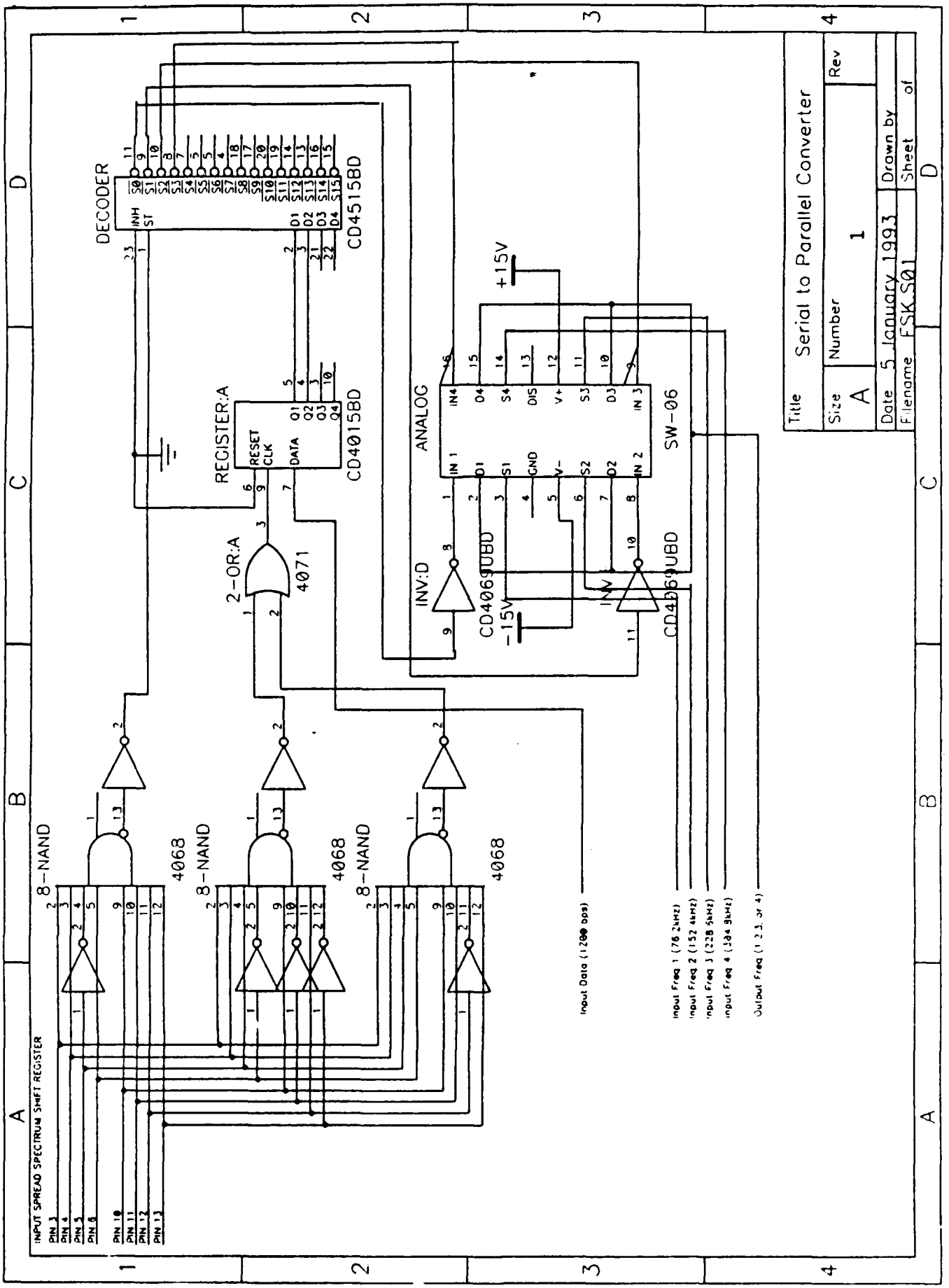
Modify the early minus late module by eliminating one-half of the envelope detectors, low pass filters summing operational amplifiers, and gain amplifier. This can be done if both early and late are switched alternately through the remaining half and then adding a sample and hold to retain these signal values for subsequent subtraction. This would result in a better balance (identical) between early and late signals, which would lock the m-sequences closer in-phase.

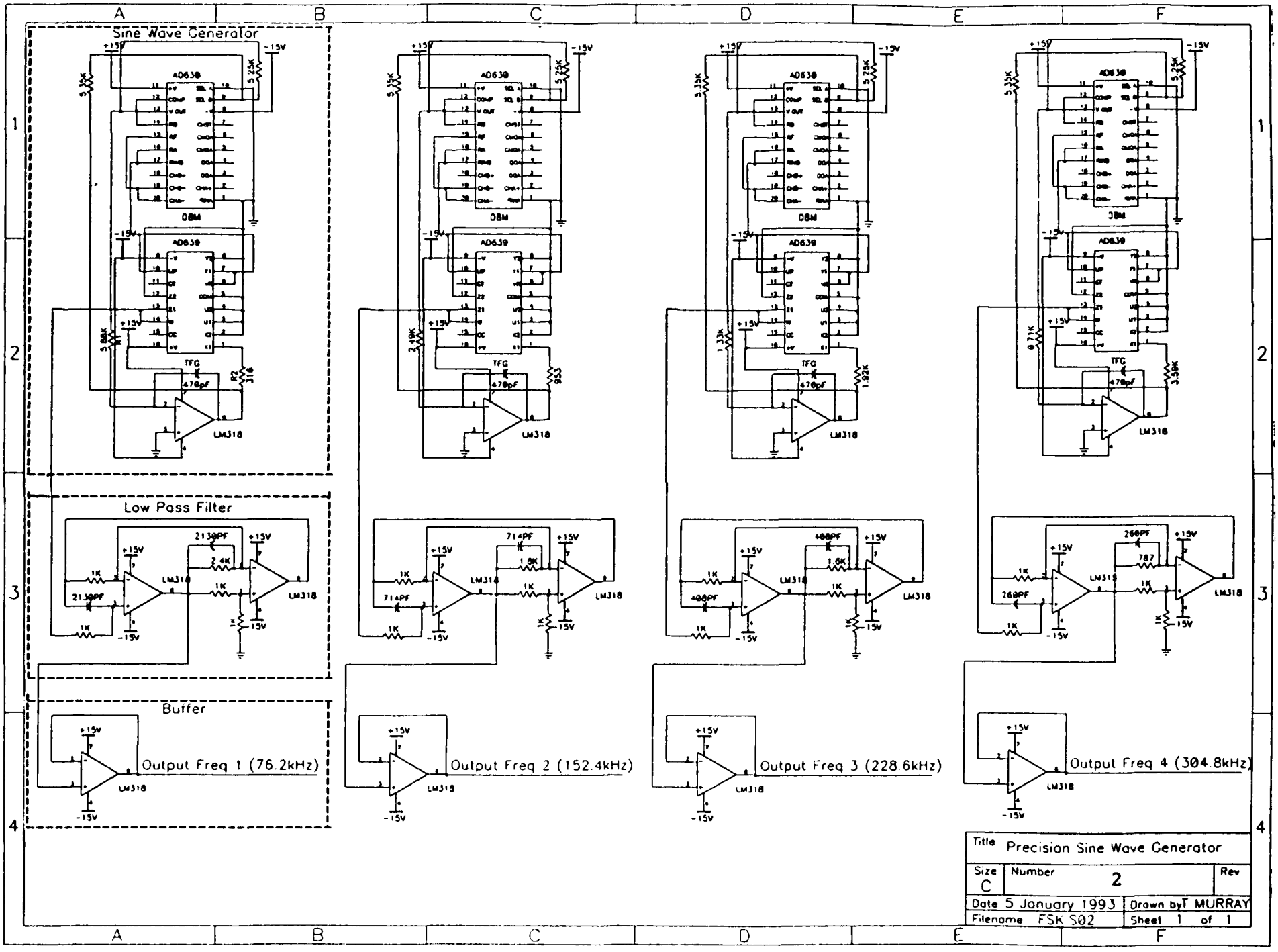
In the track module, add an integrate and dump circuit which would take the input early minus late voltage and output the average DC offset voltage. This would preclude any possibility of a false comparison with the zero volt reference voltage. The ALU can be removed if a BUS is added which would allow the communications control unit microprocessor to perform the required additions and subtractions.

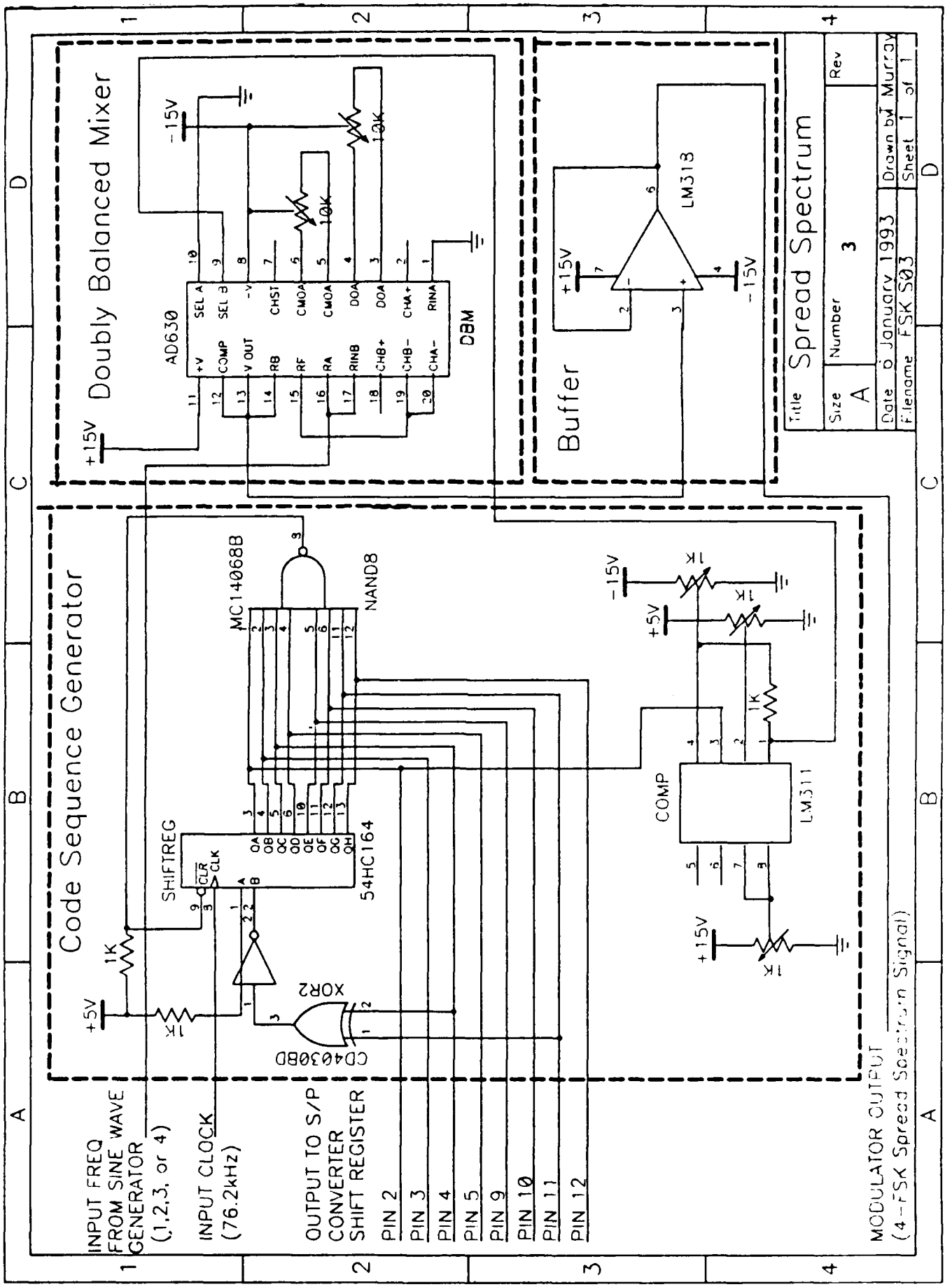
The demodulator synchronization was based on a m-sequence length of 127 with taps on the third and seventh stages. A second two tap m-sequence length of 127 exists with taps on the first and seventh stages. If the taps are changed then the synchronization code bytes must also be changed to

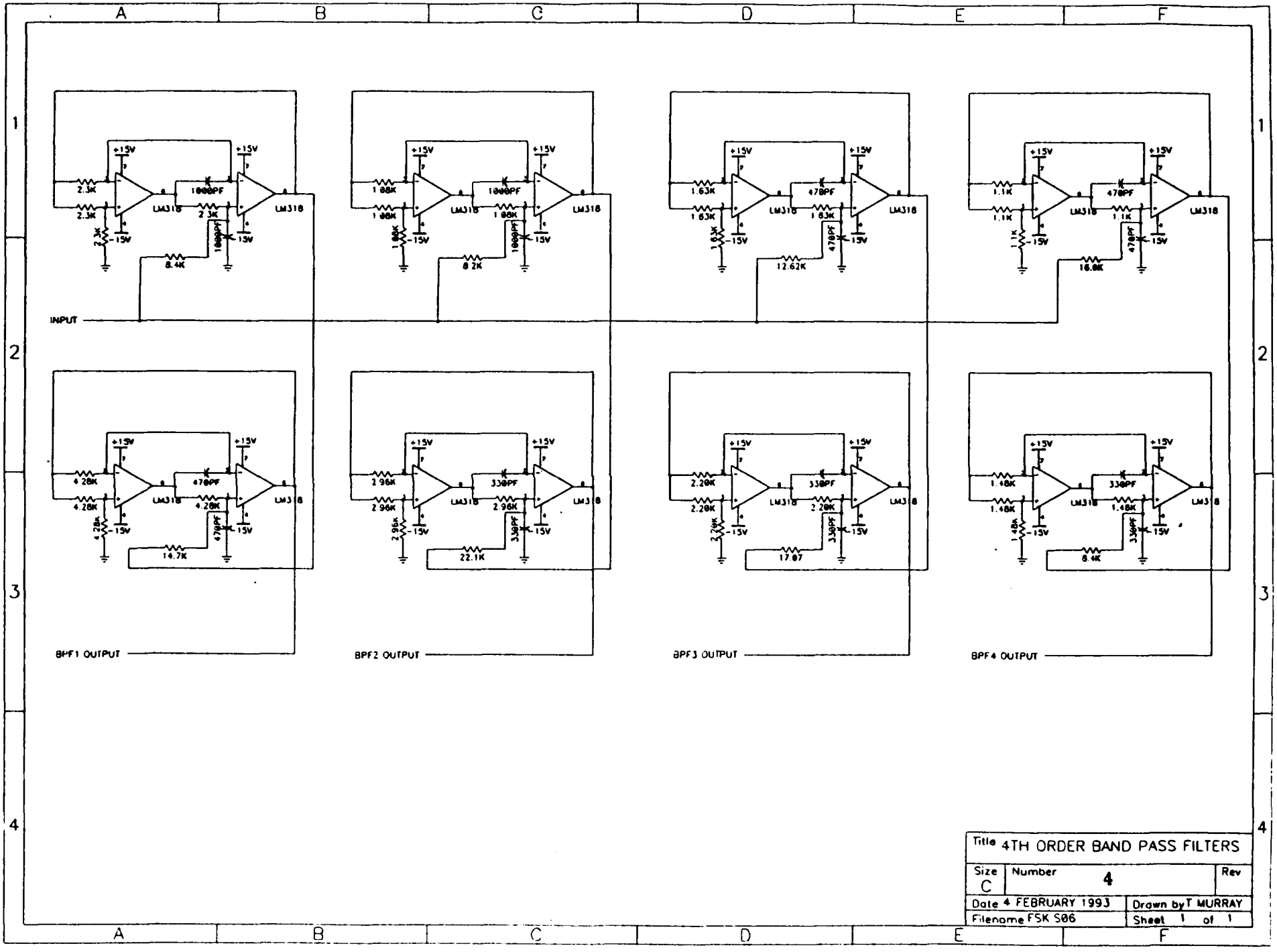
correspond to the same relative positions within the m-sequence.

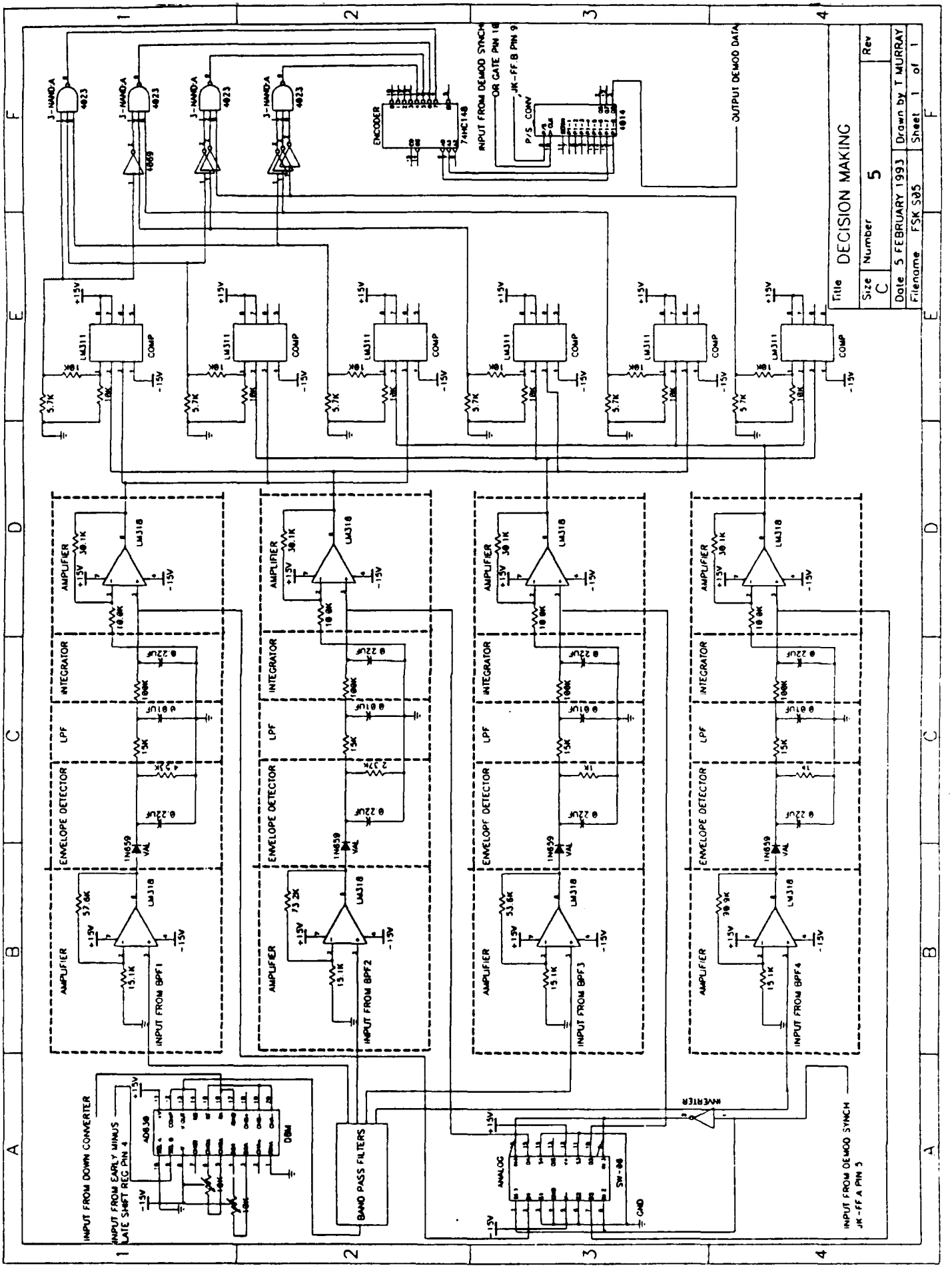
APPENDIX A: CIRCUIT SCHEMATICS

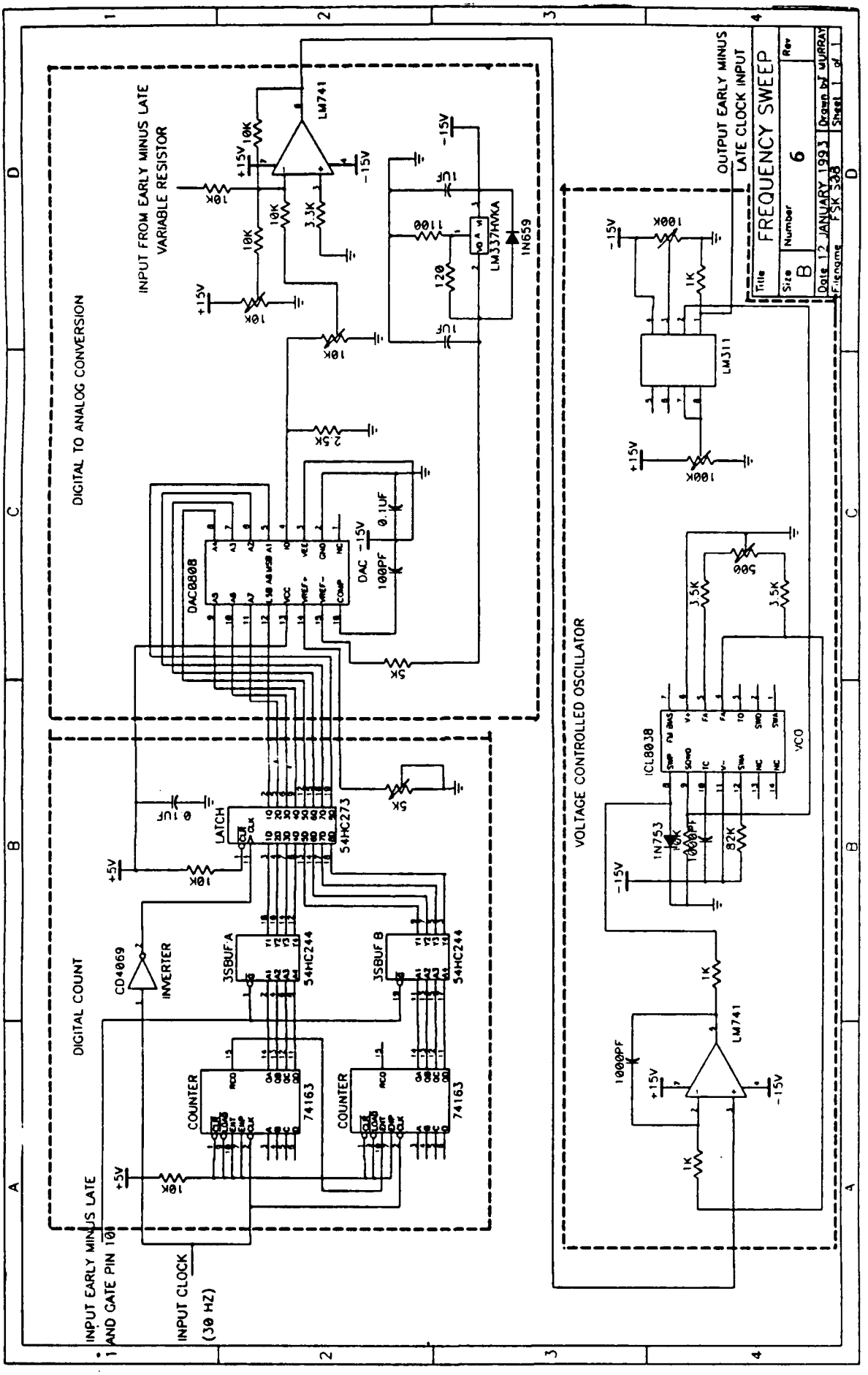

DECODER
CD4515BD
REGISTER:A
CD4015BD
2-OR:A
4071
ANALOG
SW-06
INV:D
CD4069UBD
+15V
-15V
8-NAND
4068
Input Data (1200 bps)
Input Freq 1 (76.2kHz)
Input Freq 2 (152.4kHz)
Input Freq 3 (228.6kHz)
Input Freq 4 (304.8kHz)
Output Freq (1,2,3, or 4)
INPUT SPREAD SPECTRUM SHIFT REGISTER
Title Serial to Parallel Converter
Size A
Number 1
Rev
Date 5 January 1993
Drawn by
Filename FSK.S01
Sheet of

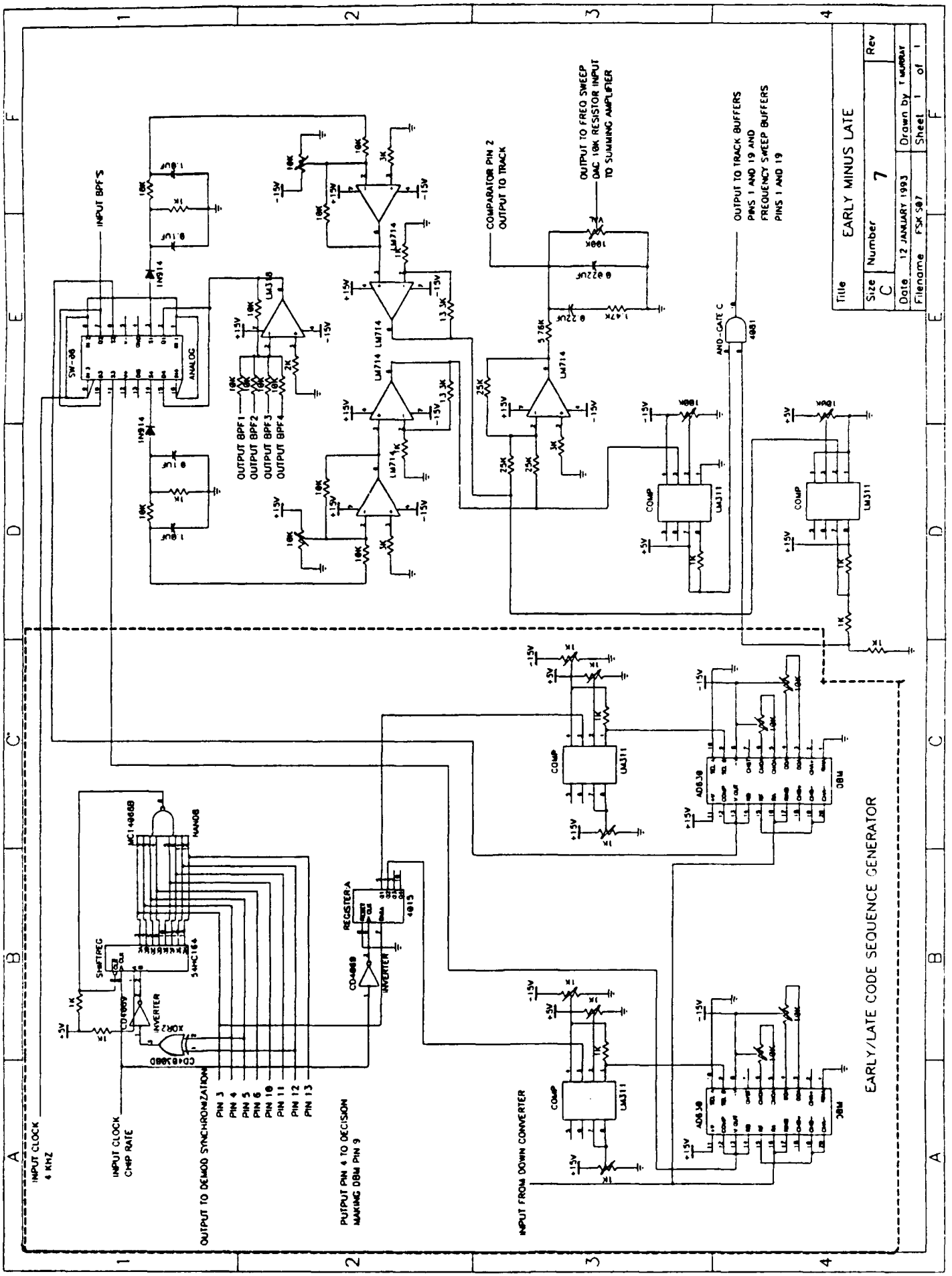

Sine Wave Generator
Low Pass Filter
Buffer
AD638
AD639
DBM
TFG
LM318
Output Freq 1 (76.2kHz)
Output Freq 2 (152.4kHz)
Output Freq 3 (228.6kHz)
Output Freq 4 (304.8kHz)
Title Precision Sine Wave Generator
Size C
Number 2
Rev
Date 5 January 1993
Drawn by T MURRAY
Filename FSK S02
Sheet 1 of 1

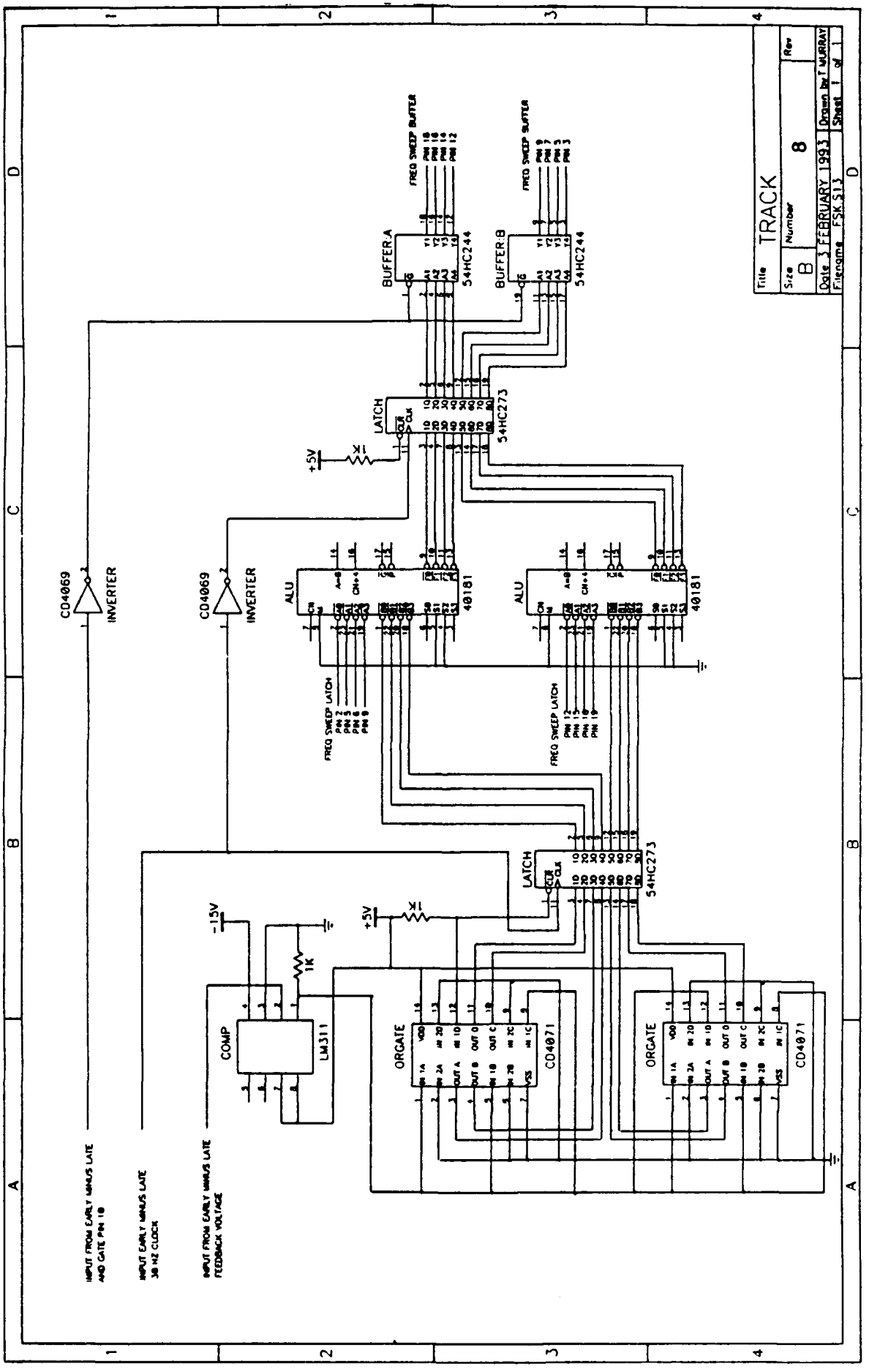

Doubly Balanced Mixer
AD630
DBM
Buffer
LM313
Spread Spectrum
Code Sequence Generator
MC14068B
NAND8
SHIFTREG
54HC164
XOR2
CD4030BD
COMP
LM311
INPUT FREQ FROM SINE WAVE GENERATOR (1,2,3, or 4)
INPUT CLOCK (76.2kHz)
OUTPUT TO S/P CONVERTER SHIFT REGISTER
PIN 2
PIN 3
PIN 4
PIN 5
PIN 9
PIN 10
PIN 11
PIN 12
MODULATOR OUTPUT (4-FSK Spread Spectrum Signal)
Title
Size A
Number 3
Rev
Date 6 January 1993
Drawn by Murray
Filename FSK S03
Sheet 1 of 1

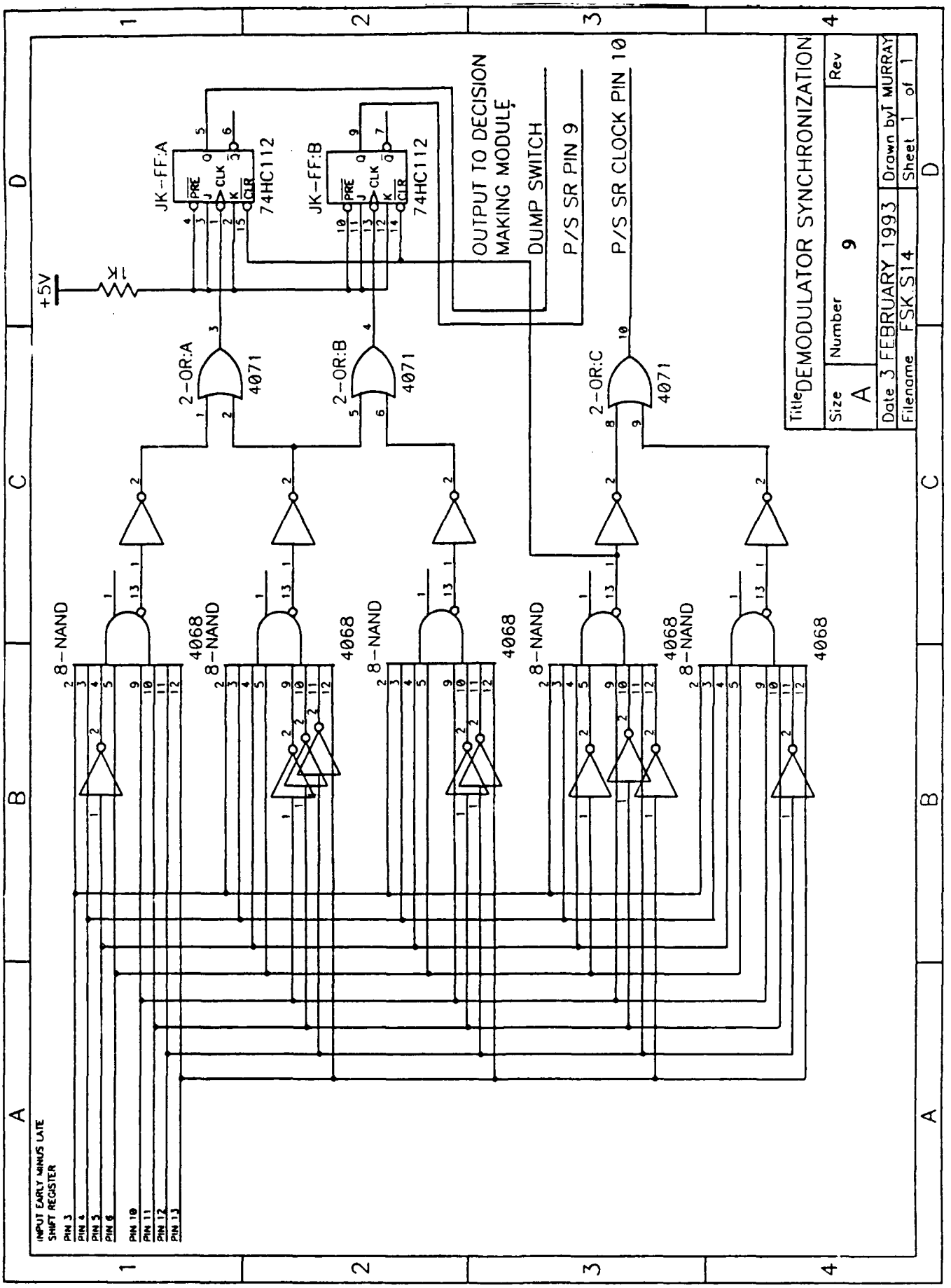

A
B
C
D
E
F
1
2
3
4
+15V
-15V
LM318
1000PF
2.3K
8.4K
8.2K
1.98K
12.62K
1.63K
470PF
16.8K
1.1K
INPUT
4.28K
14.7K
470PF
2.96K
22.1K
330PF
2.20K
17.8K
1.48K
8.4K
BPF1 OUTPUT
BPF2 OUTPUT
BPF3 OUTPUT
BPF4 OUTPUT
Title 4TH ORDER BAND PASS FILTERS
Size C
Number 4
Rev
Date 4 FEBRUARY 1993
Drawn by T MURRAY
Filename FSK S06
Sheet 1 of 1


DECISION MAKING
Size C
Number 5
Rev
Date 5 FEBRUARY 1993
Drawn by T MURRAY
Filename FSK S05
Sheet 1 of 1
OUTPUT DEMOD DATA
INPUT FROM DEMOD SYNCH
OR GATE PIN 10
JK-FF B PIN 9
ENCODER
74HC148
P/S CONV
J-NANDA
4023
4069
4016
LM311
COMP
AMPLIFIER
LM318
INTEGRATOR
LPF
ENVELOPE DETECTOR
IN659
VAL
INPUT FROM BPF1
INPUT FROM BPF2
INPUT FROM BPF3
INPUT FROM BPF4
INVERTER
BAND PASS FILTERS
INPUT FROM DOWN CONVERTER
INPUT FROM EARLY MINUS LATE SHIFT REG PIN 4
INPUT FROM DEMOD SYNCH JK-FF A PIN 5
ANALOG
SW-08
GND
DBM
+15V
-15V


DIGITAL TO ANALOG CONVERSION
INPUT FROM EARLY MINUS LATE VARIABLE RESISTOR
LM741
LM337HVKA
IN659
DAC8808
DAC -15V
0.1UF
100PF
54HC273
LATCH
DIGITAL COUNT
CD4069
INVERTER
3SBUF A
3SBUF B
54HC244
COUNTER
74163
INPUT EARLY MINUS LATE
1 AND GATE PIN 10
INPUT CLOCK
(30 HZ)
VOLTAGE CONTROLLED OSCILLATOR
OUTPUT EARLY MINUS LATE CLOCK INPUT
LM311
ICL8038
VCO
1N753
82K
1000PF
FREQUENCY SWEEP
Number 6
Date 12 JANUARY 1993
Drawn by MURRAY
Filename FSK308


EARLY MINUS LATE
Title
Number 7
Rev
Size C
Date 12 JANUARY 1993
Drawn by T MURRAY
Filename FSK S87
Sheet 1 of 1
INPUT BPF'S
OUTPUT BPF1
OUTPUT BPF2
OUTPUT BPF3
OUTPUT BPF4
COMPARATOR PIN 2 OUTPUT TO TRACK
OUTPUT TO FREQ SWEEP DAC 10K RESISTOR INPUT TO SUMMING AMPLIFIER
OUTPUT TO TRACK BUFFERS PINS 1 AND 19 AND FREQUENCY SWEEP BUFFERS PINS 1 AND 19
AND-GATE C
4081
INPUT CLOCK 4 KHZ
INPUT CLOCK CHIP RATE
OUTPUT TO DEMOD SYNCHRONIZATION
PIN 3
PIN 4
PIN 5
PIN 6
PIN 10
PIN 11
PIN 12
PIN 13
PUTPUT PIN 4 TO DECISON MAKING DBM PIN 9
INPUT FROM DOWN CONVERTER
EARLY/LATE CODE SEQUENCE GENERATOR


Title TRACK
Size B
Number 8
Rev
Date 3 FEBRUARY 1993
Drawn by T MURRAY
Filename FSK S13
Sheet 1 of 1
BUFFER:A
BUFFER:B
54HC244
FREQ SWEEP BUFFER
LATCH
54HC273
CD4069
INVERTER
ALU
40181
FREQ SWEEP LATCH
-15V
+5V
1K
COMP
LM311
ORGATE
CD4071
INPUT FROM EARLY MINUS LATE AND GATE PIN 10
INPUT EARLY MINUS LATE 38 Hz CLOCK
INPUT FROM EARLY MINUS LATE FEEDBACK VOLTAGE


JK-FF:A
74HC112
JK-FF:B
74HC112
+5V
OUTPUT TO DECISION MAKING MODULE
DUMP SWITCH
P/S SR PIN 9
P/S SR CLOCK PIN 10
2-OR:A
4071
2-OR:B
4071
2-OR:C
4071
8-NAND
4068
INPUT EARLY MINUS LATE SHIFT REGISTER
PIN 3
PIN 4
PIN 5
PIN 6
PIN 10
PIN 11
PIN 12
PIN 13
Title DEMODULATOR SYNCHRONIZATION
Size A
Number 9
Rev
Date 3 FEBRUARY 1993
Drawn by MURRAY
Filename FSK.S14
Sheet 1 of 1

APPENDIX B: GENERALIZED IMPEDANCE CONVERTER (GIC) FILTER DESIGN

The GIC was selected for the active filter design because it eliminates the need for inductors, has superior sensitivity characteristics, and 20dB per decade attenuation outside the pass band per each two operational amplifier, eight passive element stage. The GIC information contained in this Appendix was extracted from [Ref. 11:pp. 18-22] which should be reviewed for additional details.

Drawing B-1 is a diagram of the GIC where the Y represents the impedance of one or two passive elements and T represents the transfer function at that circuit node. Two values of T are identified, T_1 for the transfer function of a band pass filter and T_2 for the transfer function of low pass filter. The GIC is capable of implementing high pass, notch, and all pass filters, but these are not discussed since they were not used in this thesis. The non-ideal (operational amplifiers modeled by a single pole) transfer function of the GIC at output nodes T_1 and T_2 are

$$T_1\ NUMERATOR = \frac{(Y_1+Y_3)(Y_2+Y_5+Y_6)Y_7}{A_1} + (Y_2+Y_6)(Y_3Y_7) + Y_1Y_4Y_5 - Y_3Y_5Y_8$$

$$T_1\ DENOMINATOR = \frac{(Y_4+Y_7+Y_8)(Y_1+Y_3)(Y_2+Y_5+Y_6)}{A_1A_2} + \frac{(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)Y_1}{A_1}$$

$$+ \frac{(Y_4+Y_7+Y_8)(Y_2+Y_5+Y'Y_3}{A_2} + (Y_7+Y_8)(Y_2Y_3) + (Y_5+Y_6)(Y_1Y_4)$$

$$T_2\ NUMERATOR = \frac{(Y_4+Y_7+Y_8)(Y_1+Y_3)Y_5}{A_2} + (Y_4+Y_8)Y_1Y_5 + Y_2Y_3Y_7 + Y_1Y_6Y_7$$

$$T_2\ DENOMINATOR = T_1\ DENOMINATOR$$

To create a band pass filter use transfer function T_1 and set $Y_1=Y_2=Y_4=Y_6=G$, $Y_3=Y_8=C$, and $Y_7=G/Q$ where G is admittance, C is capacitance, and Q is the quality factor of the filter. The actual values of G(1/R) and C are calculated from the equation for the band pass filter's center frequency (W_0)

$$\omega_0 = \frac{1}{RC}$$

The Q of the filter is calculated using the center frequency and the upper and lower 3dB frequencies (W_u and W_l respectively).

$$Q = \frac{\omega}{\omega_u - \omega_l}$$

Observe that the transfer functions contain terms divided by the small signal bandwidth (A). For ideal filters "A" approaches infinity and these terms approach zero. The equation used to calculate ω_0 assumes that ideal operational amplifiers are used to construct the filter, this is not the case in practice. As the frequency increases the denominator of the small signal bandwidth terms no longer dominates and the magnitude of the transfer function becomes less than the idealized model. The net result is that the idealized band pass filter shifts down in frequency and passes a band of frequencies less than designed for using the equations for ω_0 and Q.

To correct for an operational amplifier's finite small signal bandwidth, use the following procedure (test results were quite accurate):

1. Choose operational amplifiers with a relatively wide small signal bandwidth and fast slew rate. (The design of all active filters in this thesis used LM318 operational amplifiers which have a small signal bandwidth of 15 MHz and a slew rate of 70 volts per microsecond.)

2. Using the Matlab program for plotting the non-ideal GIC band pass filter transfer function (T1) provided in Appendix E, enter the range of frequencies of interest (w) in radians, the center frequency (w0), and the Q of the filter.

3. Plot the non-ideal transfer function and calculate from the plot how far down in frequency the center frequency shifted from the required center frequency.

4. Add this amount to the center frequency (w0) in the Matlab program.

5. After only a few iterations, the plot of the band pass filter will meet the filter design specifications.

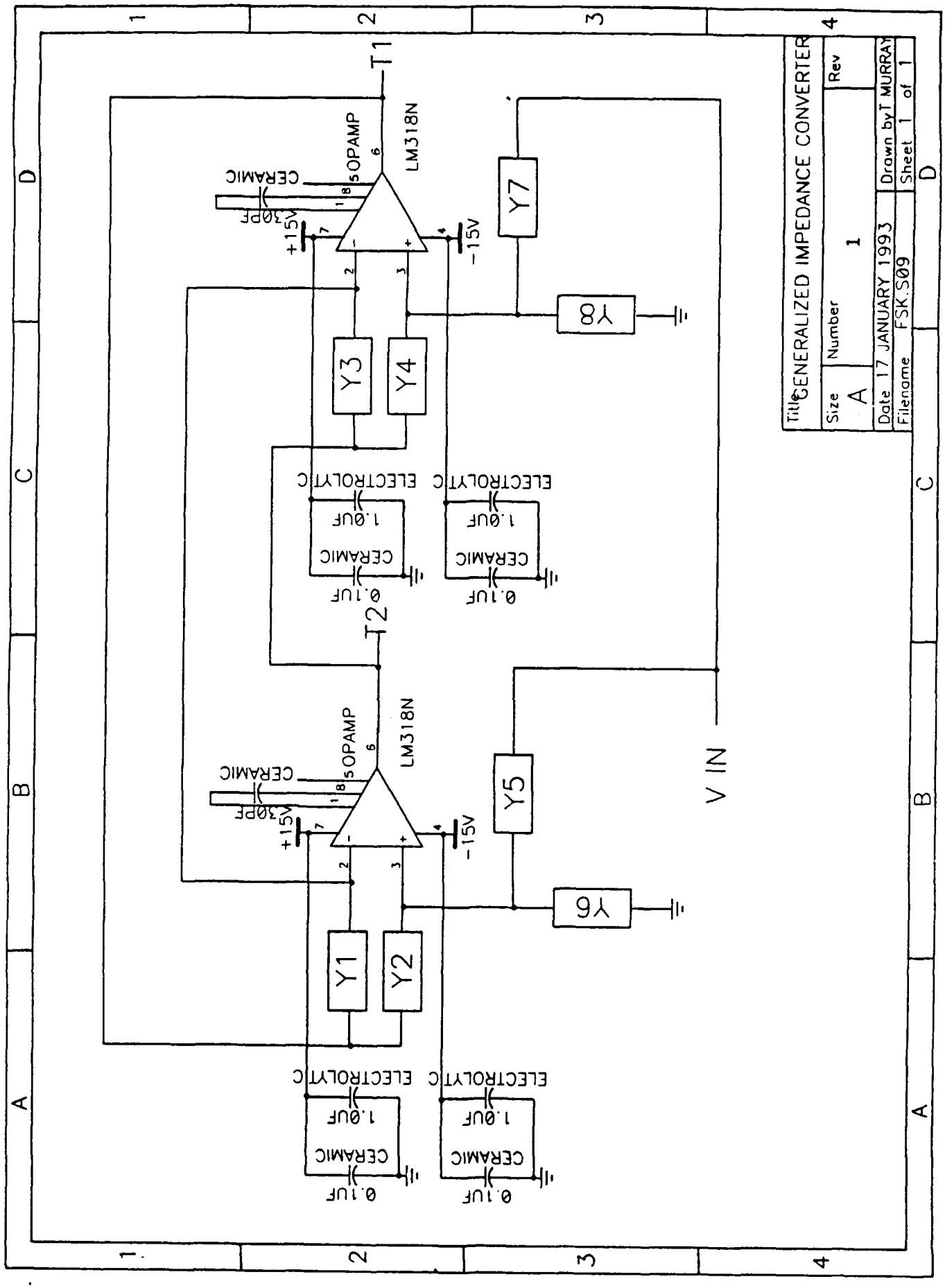
6. The ratio of the passive element values can now be calculated from the equation

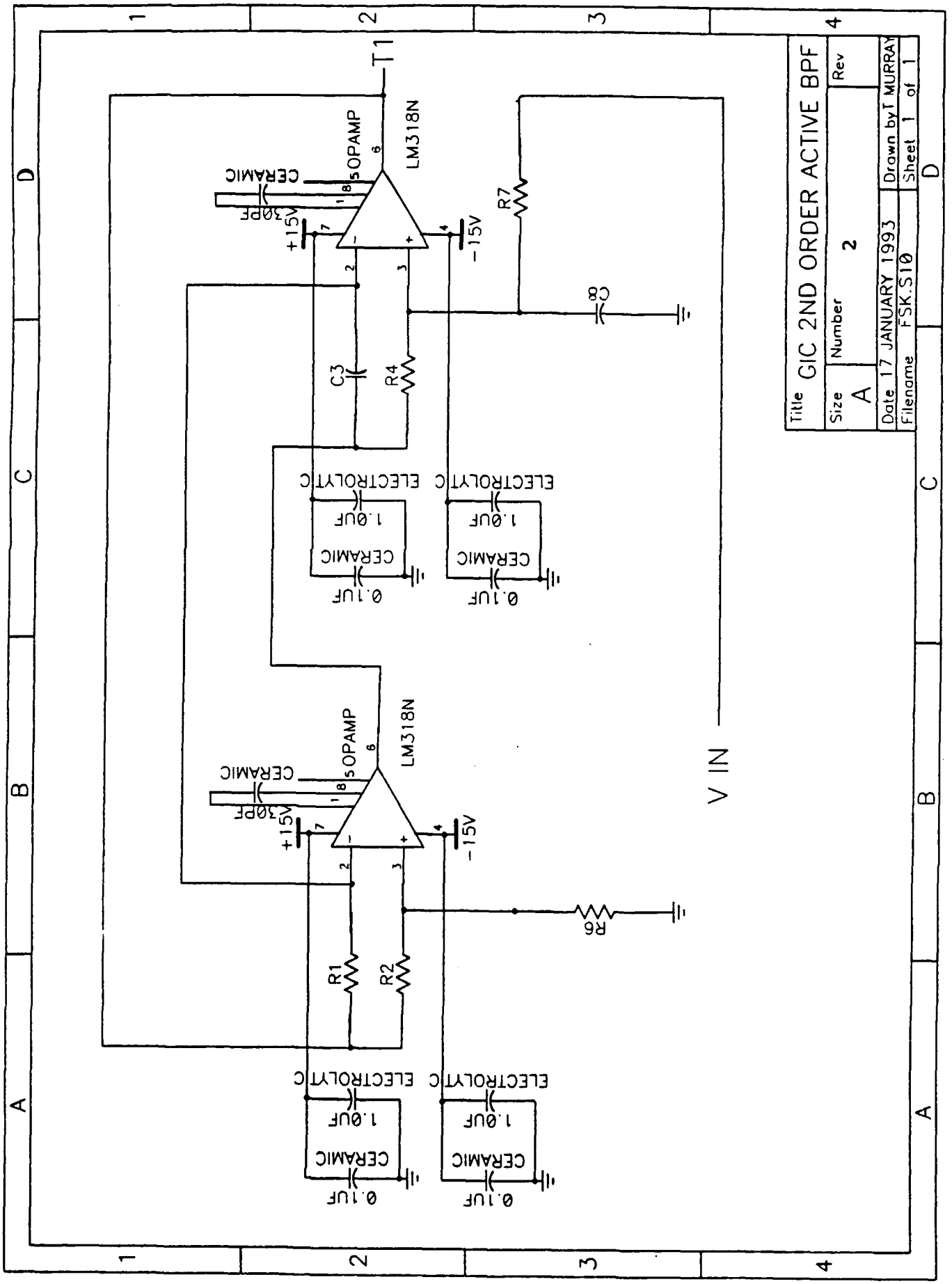
$$\omega_0' = \frac{1}{RC}$$

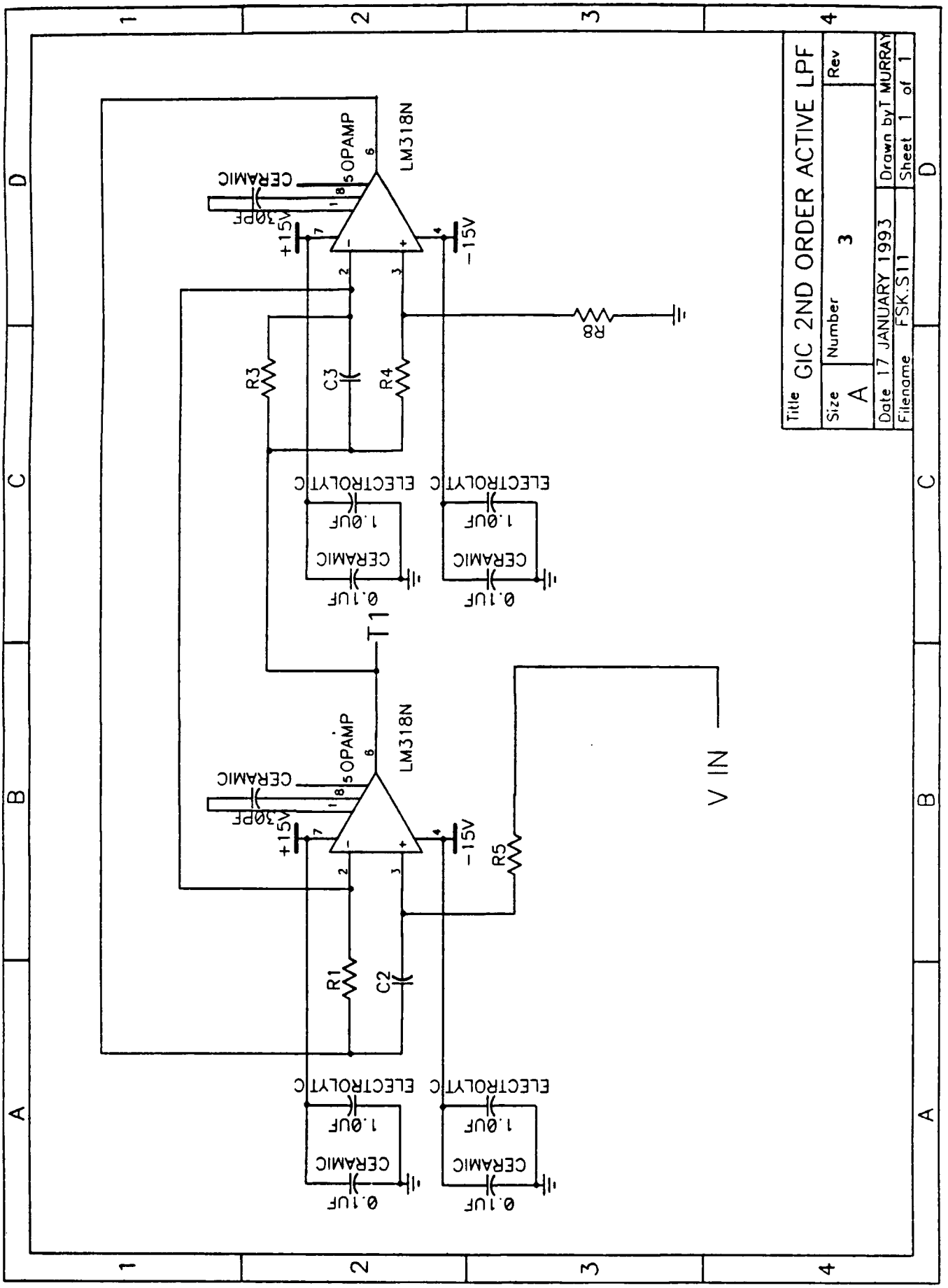
where ω_0' is the adjusted center frequency. Choose R and C based on availability.

7. Construct the band pass filter circuit of Drawing B-2.

For low pass filter design use the same steps as for a band pass filter, only replace transfer function T_2 for T_1. Use the Matlab program provided in Appendix E and construct the low pass filter of Drawing B-3.

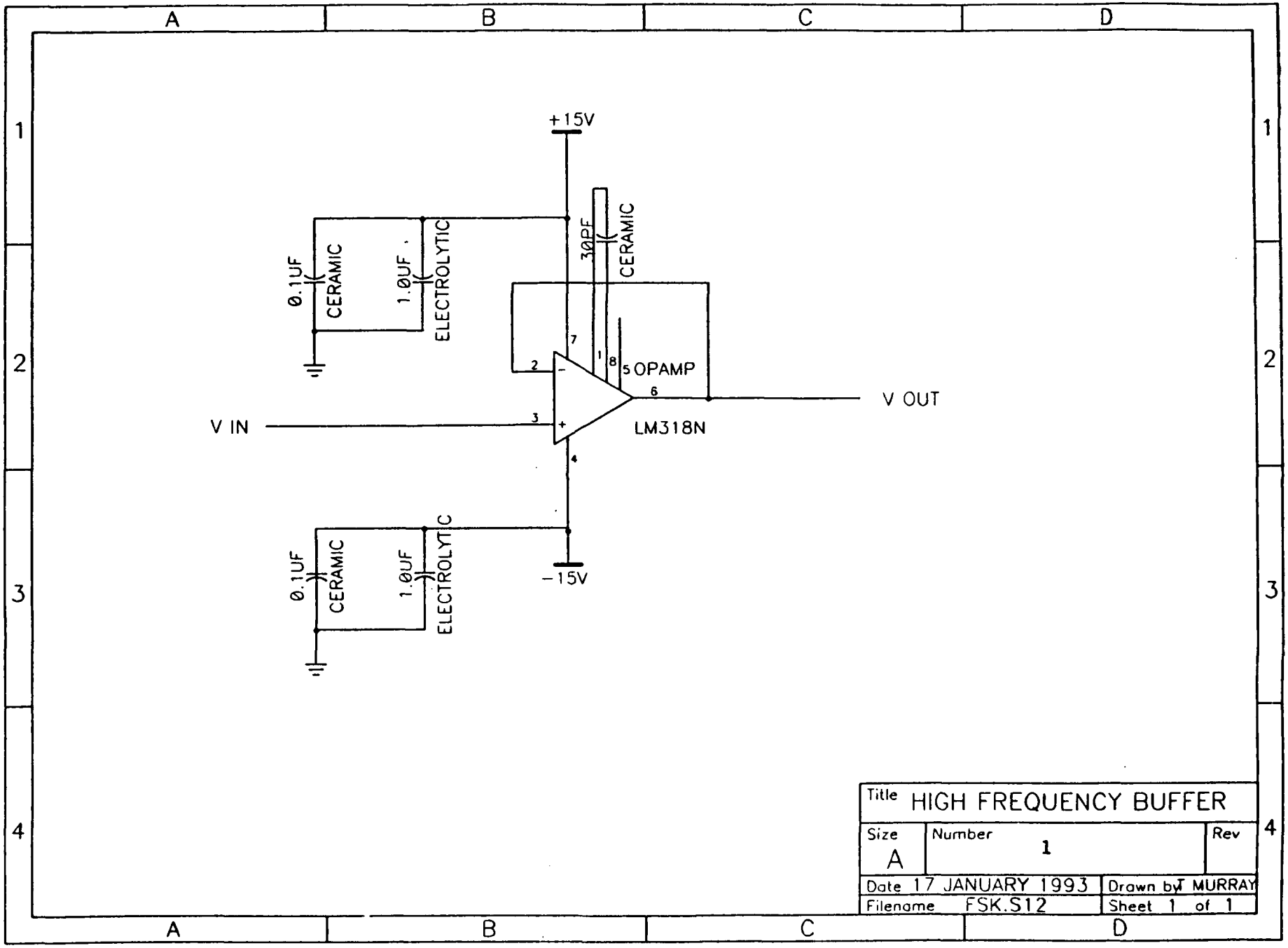

GENERALIZED IMPEDANCE CONVERTER
Title
Size A
Number 1
Rev
Date 17 JANUARY 1993
Drawn by T MURRAY
Filename FSK_S09
Sheet 1 of 1
T1
T2
LM318N
SOPAMP
CERAMIC
30PF
+15V
-15V
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
ELECTROLYTIC
1.0UF
0.1UF
V IN


T1
LM318N
OPAMP
CERAMIC
30PF
+15V
-15V
R7
C3
R4
C8
ELECTROLYTIC
1.0UF
0.1UF
V IN
R6
R1
R2
Title GIC 2ND ORDER ACTIVE BPF
Size A
Number 2
Rev
Date 17 JANUARY 1993
Drawn by T MURRAY
Filename FSK.S10
Sheet 1 of 1


Title GIC 2ND ORDER ACTIVE LPF
Size A
Number 3
Rev
Date 17 JANUARY 1993
Drawn by T MURRAY
Filename FSK.S11
Sheet 1 of 1
LM318N
OPAMP
CERAMIC
30PF
+15V
-15V
R1
R2
R3
R4
R5
R8
C2
C3
ELECTROLYTIC
1.0UF
0.1UF
T1
V IN

APPENDIX C: BUFFERS

High frequency buffers are used throughout this design. Each buffer was designed to isolate components which would otherwise not function properly when connected together due to impedance mismatch. This is accomplished by the use of LM318 operational amplifiers constructed as in Drawing C-1. A 0.1 μF ceramic and a 1.0 μF electrolytic capacitor are placed near the positive and negative power supplies to bypass high frequency signals. A 30 pF ceramic capacitor is placed between the decompensation pins (1 and 5) to extend the gain-bandwidth product. Buffers built without the power supply bypass capacitors and decompensation capacitor were extremely unstable even at low frequencies (below 1KHz).


A
B
C
D
1
2
3
4
+15V
0.1UF
CERAMIC
1.0UF
ELECTROLYTIC
30PF
CERAMIC
7
1
8
5 OPAMP
2
6
V OUT
V IN
3
LM318N
4
0.1UF
CERAMIC
1.0UF
ELECTROLYTIC
-15V
Title HIGH FREQUENCY BUFFER
Size A
Number 1
Rev
Date 17 JANUARY 1993
Drawn by J MURRAY
Filename FSK.S12
Sheet 1 of 1

APPENDIX D: DOPPLER SHIFT

Worst case doppler shift calculations were based on the following assumptions:

1. The earth is spherical with a constant radius.

2. The azimuth angle between the satellite and the position on earth is equal to zero; only the elevation angle changes.

3. The satellite elevation above the earth (a) is constant.

Using the law of cosines and Figure D-1, the slant range as a function of time, a(t), is equal to:

$$a^2(t) = R^2+r^2-2Rr\cos\theta(t)$$

$$a(t) = \sqrt{R^2+r^2-2Rr\cos\theta(t)}$$

where R (radius of earth) = 6373 km

r (radius of satellite orbit) = 7113.8 km

To find the change in slant range as a function of time, take the first derivative of a(t).

$$\frac{d}{dt}a(t) = \frac{Rr\sin\theta}{\sqrt{R^2+r^2-2Rr\cos\theta}}\frac{d}{dt}\theta$$

Substituting the orbital velocity (V) for $rd\theta/dt$ in the previous equation and knowing the velocity of a circular orbit is equal to:

$$V = \sqrt{\frac{GM}{r}}$$

the equation for the relative velocity between a satellite and a fixed position on earth given the assumptions stated above is:

$$\frac{d}{dt}a(t) = \frac{R\sqrt{\frac{GM}{r}}\sin\theta}{\sqrt{R^2+r^2-2Rr\cos\theta}}$$

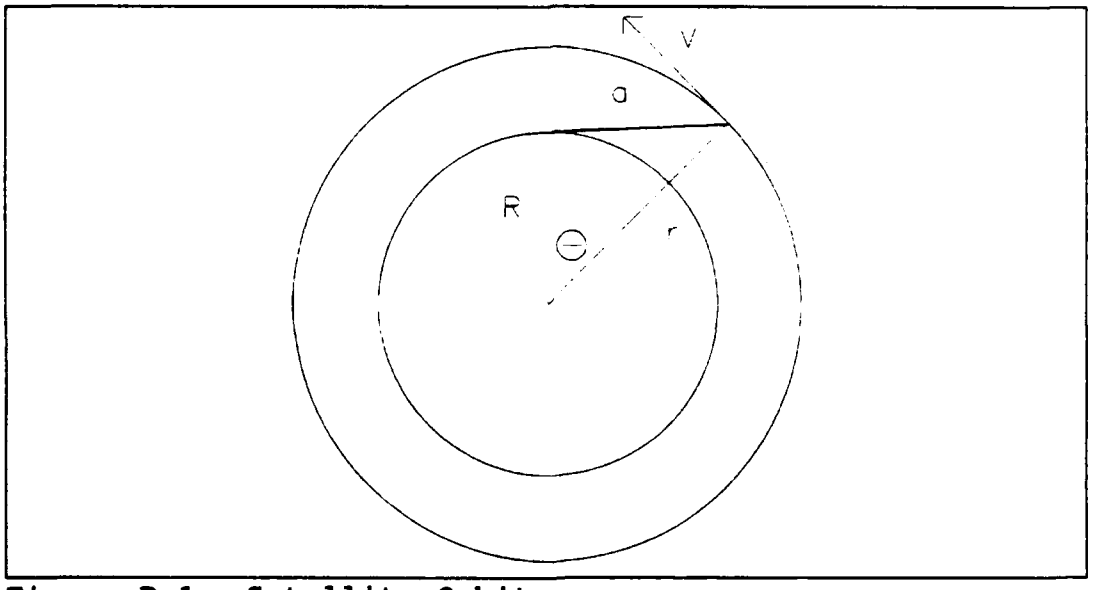


Figure D-1. Satellite Orbit

where G (Gravitational constant) = 6.67×10^{-11} Nm^2/kg^2

M (Mass of the earth) = 5.98×10^{24} kg

A plot of relative slant range velocity (u) versus elevation angle is shown in Figure D-2.

Knowing the maximum relative slant range velocity (u_{max}) from Figure D-2 and the equation for doppler shift,

$$f^1 = \frac{f}{1 - \frac{u}{c}\cos\theta}$$

the maximum shift in channel frequency (f^1_{max}) can be calculated from:

$$f^1_{max} = \frac{f_c - f_n}{1 - \frac{u_{max}}{c}\cos\theta_{min}}$$

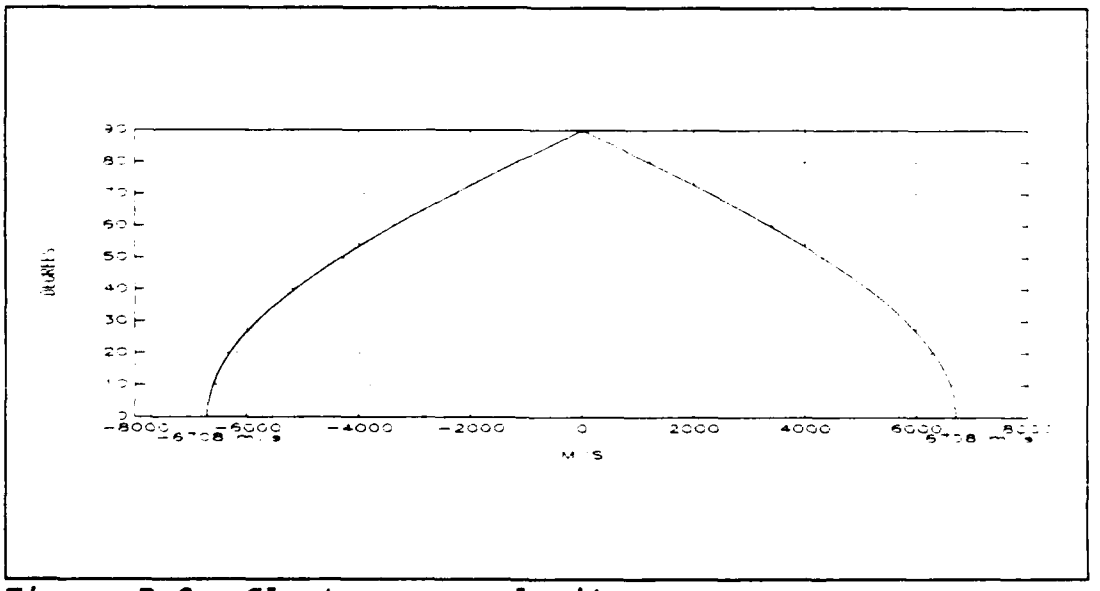


Figure D-2. Slant range velocity

where f_c (Carrier frequency) = 437.25 MHz

f_4 (Highest baseband frequency) = 304.8 kHz

u_{max} (Maximum slant range velocity) = 6708 m/s

c (Speed of light) = 3×10^8 m/s

θ_{min} (Minimum elevation angle) = 0 degrees

The maximum doppler shift in frequency is equal to ±9784 Hz. A plot of the channel frequency shift caused by the doppler effect versus the elevation angle of the satellite with respect to the horizon is shown in Figure D-3. The MATLAB code used to create these plots is provided in Appendix E.

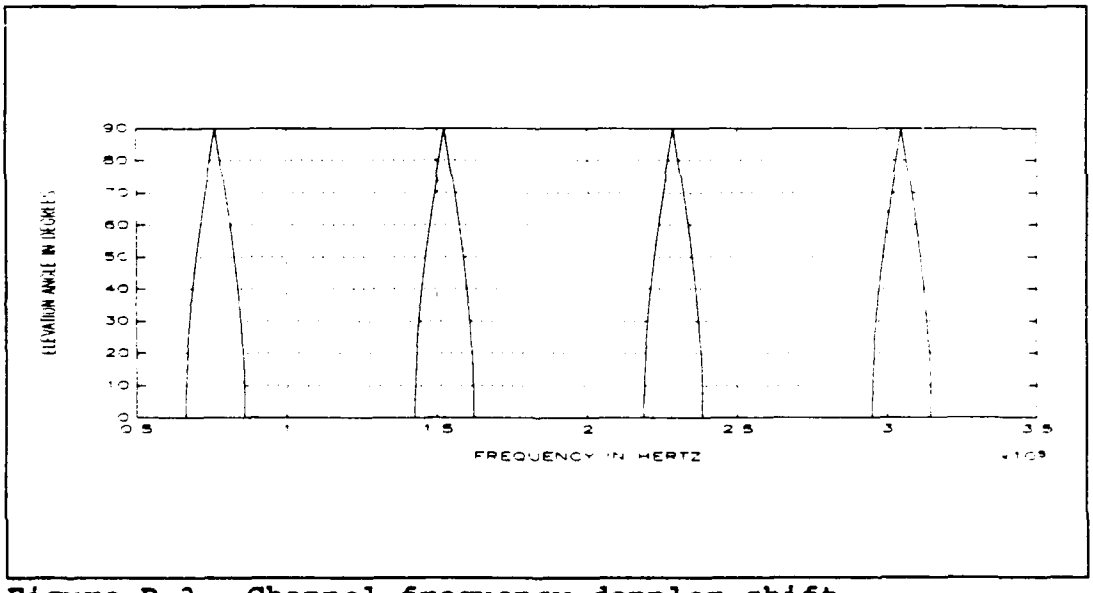


Figure D-3. Channel frequency doppler shift

APPENDIX E: COMPUTER PROGRAMS

```
%Band Pass Filter Design (filename th008.m)
%The variables used in this example were for the center frequency
%equal to  76.2 kHz and 3db frequencies of +/- 10.4 kHz
!del th008a.met
!del th008b.met
!cls
clear
clg
w = 2*pi*20e3:500:2*pi*140e3;    %range of frequencies plotted
s = j*w;
wt1 = 2*pi*15e6;                 %enter small signal bandwidth of the
wt2 = 2*pi*15e6;                 %opamps used to construct filter
w01 = 2*pi*69230;                %enter center frequency of first stage
Q = 3.6634;                      %enter Q of the filter
R = 1000;                        %nominal resistance value
C = (R*w01)^(-1);                %capacitance
G = R^(-1);                      %admittance
A1 = wt1./s;
A2 = wt2./s;
Y1 = G;
Y2 = G;
Y3 = C*s;
Y4 = G;
Y5 = 0;
Y6 = G;
Y8 = C*s;
Y7 = G/Q;
J  = Y4+Y7+Y8;
K  = Y1+Y3;
L  = Y2+Y5+Y6;
%
NUM = ((K.*L.*Y7)./A1)+((Y2+Y6).*Y3.*Y7)+(Y1.*Y4.*Y5)...
      -(Y3.*Y5.*Y8);
DEN = ((J.*K.*L)./(A1.*A2))+((J.*L.*Y1)./A1)+((J.*L.*Y3)./A2) ...
      +((Y7+Y8).*Y2.*Y3)+((Y5+Y6).*Y1.*Y4);
T1 = (NUM./DEN);
T1a = sqrt((real(T1)).^2+(imag(T1)).^2);
%
R = 1000;                        %enter resistance
w02 = 2*pi*84034;                %enter center frequency of second stage
C = (R*w02)^(-1);
G = R^(-1);
A1 = wt1./s;
A2 = wt2./s;
Y1 = G;
Y2 = G;
Y3 = C*s;
Y4 = G;
Y5 = 0;
Y6 = G;
Y8 = C*s;
Y7 = G/Q;
J  = Y4+Y7+Y8;
K  = Y1+Y3;
L  = Y2+Y5+Y6;
%
NUM = ((K.*L.*Y7)./A1)+((Y2+Y6).*Y3.*Y7)+(Y1.*Y4.*Y5)...
      -(Y3.*Y5.*Y8);
DEN = ((J.*K.*L)./(A1.*A2))+((J.*L.*Y1)./A1)+((J.*L.*Y3)./A2) ...
      +((Y7+Y8).*Y2.*Y3)+((Y5+Y6).*Y1.*Y4);
```

```
T2 = (NUM./DEN);
T2a = sqrt((real(T2)).^2+(imag(T2)).^2);
x = [65.8e3 65.8e3 86.6e3 86.6e3];
y = [-5 5.455 5.455 -5];
plot(w/(2*pi),20*log10(T1a),w/(2*pi),20*log10(T2a),x,y);
%title('4th ORDER BPF, f0=76.2k, Q=3.6634');
xlabel('FREQ HZ');
ylabel('MAGNITUDE dB');
grid
meta th008a
T12 = T1.*T2;
T12a = sqrt((real(T12)).^2+(imag(T12)).^2);
plot(w/(2*pi),20*log10(T12a),x,y);
%title('4th ORDER BPF, f0=76.2k, Q=3.6634');
xlabel('FREQ HZ');
ylabel('MAGNITUDE dB');
grid
meta th008b
```

```
%Low Pass Filter Design (filename thlp1.m)
%The variables used in this example were for a 3dB frequency of 100 kHz
!del thlp1a.met
!cls
clear
clg
w = 1:1000:1256.6e3;    %range of frequencies plotted
s = j*w;
wt1 = 2*pi*1e6;         %enter small signal bandwidth of the
wt2 = 2*pi*1e6;         %opamps used to construct the filter
R = 4444;               %nominal resistance value
w0 = 2*pi*100e3;        %enter the center frequency
Q = 2.4;                %enter Q of the filter
C = (R*w0)^(-1);        %capacitance
G = R^(-1);             %admittance
A1 = wt1./s;
A2 = wt2./s;
Y1 = G;
Y2 = C*s;
Y3 = C*s+G/Q;
Y4 = G;
Y5 = G;
Y6 = 0;
Y7 = 0;
Y8 = G;
J  = Y4+Y7+Y8;
K  = Y1+Y3;
L  = Y2+Y5+Y6;
%
NUM = ((K.*J.*Y5)./A2)+((Y4+Y8).*Y1.*Y5)+(Y2.*Y3.*Y7)-(Y1.*Y6.*Y7);
DEN = ((J.*K.*L)./(A1.*A2))+((J.*L.*Y1)./A1)+((J.*L.*Y3)./A2)...
      +((Y7+Y8).*Y2.*Y3)+((Y5+Y6).*Y1.*Y4);
T = NUM./DEN;
T2 = sqrt((real(T)).^2+(imag(T)).^2);
plot(w/(2*pi),20*log10(T2));
title('LPF  f0=100KHz, Q=2.4');
xlabel('FREQ Hz');
ylabel('MAGNITUDE dB');
grid
meta thlp1a
```

```
%Doppler Shift (filename th001.m)
!del th001a.met
!del th001b.met
!cls
clear
clg
f1 = 76.2e3;                                %first frequency
f2 = 152.4e3;                               %second frequency
f3 = 228.6e3;                               %third frequency
f4 = 304.8e3;                               %fourth frequency
fc = 437.25e6;                              %carrier frequency
c = 3e8;                    % m/s           speed of light
G = 6.67e-11;               % N*m^2/kg^2    gravitational constant
M = 5.98e24;                % kg            earth mass
R = 6.373e6;                % m             earth radius
amin = 7.408e5;             % m             satellite orbital height
theta = -0.46:pi/18000:0.46;                %as shown on Figure D-1
r = R + amin;                               %as shown on Figure D-1
v = sqrt(G*M/r);                            %velocity in circular orbit
%
a =sqrt(R^2+r^2-(2*R*r*cos(theta)));  %as shown on Figure D-1
elev =(acos((R^2+a.^2-r^2)./(2*a*R))-(pi/2))*(180/pi);
dera = (R*v*sin(theta))./(sqrt(R^2+r^2-2*R*r*cos(theta)));
plot(dera,elev);
grid
%title('RELATIVE SATELLITE VELOCITY VS ELEVATION ANGLE');
xlabel('M/S');
ylabel('DEGREES');
maxdera = max(dera);
gtext('6708 m/s');
gtext('-6708 m/s');
meta th001a
clg
f1mp = (fc+f1)./(1-(dera./c));      % doppler shifted carrier/signal vector
f2mp = (fc+f2)./(1-(dera./c));
f3mp = (fc+f3)./(1-(dera./c));
f4mp = (fc+f4)./(1-(dera./c));
rf1 = f1mp-fc;                      % doppler shifted baseband signal vector
rf2 = f2mp-fc;
rf3 = f3mp-fc;
rf4 = f4mp-fc;
plot(rf1,elev,rf2,elev,rf3,elev,rf4,elev);
grid
title('DOPPLER FREQUENCY SHIFT RANGE');
xlabel('FREQUENCY IN HERTZ');
ylabel('ELEVATION ANGLE IN DEGREES');
meta th001b
minmax=[min(rf1) max(rf1) min(rf2) max(rf2) min(rf3) max(rf3) ...
        min(rf4) max(rf4)];         % minimum and maximum frequencies for
                                    % each FSK frequency
```

LIST OF REFERENCES

[1] Taub, H., *Digital Circuits and Microprocessors*, McGraw-Hill Book Co., 1982.

[2] Coughlin, R., and Driscoll, F., *Operational Amplifiers & Linear Integrated Circuits*, 4th ed., Prentice-Hall, Inc., 1991.

[3] Dixon, R., *Spread Spectrum Systems*, 2d ed., John Wiley & Sons., Inc., 1984.

[4] Couch, L. II, *Digital and Analog Communication Systems*, Macmillan Publishing Co., 3d ed., 1990.

[5] Haykin, S., *An Introduction to Analog and Digital Communications*, John Wiley & Sons., Inc., 1989.

[6] Ziemer, R., and Peterson, R., *Digital Communications and Spread Spectrum Systems*, Macmillan Publishing Co., 1985.

[7] Analog Devices, *Universal Trigonometric Function Generator, AD639, Specifications and Applications*, not dated.

[8] Hutchinson, C., and Kleinman, J., editors, *The ARRL Handbook for the Radio Amateur*, The American Radio League, Newton, Connecticut, 1992.

[9] *Linear and Interface Integrated Circuits*, Motorola, Inc., 1990.

[10] Analog Devices, *Balanced Modulator/Demodulator, AD630, Specifications and Applications*, not dated.

[11] Michael, S., and Andresakis, P., *Digitally Controlled Programmable Active Filters*, Proceedings of Nineteenth Annual Asilomar Conference on Circuits, Systems, and Computers, Pacific Grove, California, November, 1990.

[12] Horowitz, P., and Hill, W., *The Art of Electronics*, Cambridge University Press, 2d ed., 1989.

[13] Nillson, J., *Electric Circuits*, Addison-Wesley Publishing Co., 3d ed., 1990.

INITIAL DISTRIBUTION LIST

Defense Technical Information Center Cameron Station Alexandria, VA 22304-6145	2
Library, Code 52 Naval Postgraduate School Monterey, CA 93943-5000	2
Chairman, Code EC Department of Electical and Computer Engineering Naval Postgraduate School Monterey, CA 93943-5000	1
Professor Tri T. Ha, Code EC/Ha Department of Electical and Computer Engineering Naval Postgraduate School Monterey, CA 93943-5000	1
Professor Rudolf Panholzer, Code SP/Pz Space Systems Academic Group Naval Postgraduate School Monterey, CA 93943-5000	2
Lcdr. Terrence J. Murray 8428 Wicklow Avenue Cincinnati, OH 45236	2